

# BSP12-0001-1x

## 10 G Communication & Control Card Layer Stackup

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## 1. 8-Layer PCB Stackup

Copper (0.5 OZ, 17.5 $\mu\text{m}$ )	TOP
Prepreg (120 $\mu\text{m}$ )	
Copper (1 OZ, 35 $\mu\text{m}$ )	GNDT
Core (250 $\mu\text{m}$ )	
Copper (1 OZ, 35 $\mu\text{m}$ )	INTT
Prepreg (200 $\mu\text{m}$ )	
Copper (1 OZ, 35 $\mu\text{m}$ )	PWRT
Core (250 $\mu\text{m}$ )	
Copper (1 OZ, 35 $\mu\text{m}$ )	PWRB
Prepreg (200 $\mu\text{m}$ )	
Copper (1 OZ, 35 $\mu\text{m}$ )	INTB
Core (250 $\mu\text{m}$ )	
Copper (1 OZ, 35 $\mu\text{m}$ )	GNDB
Prepreg (120 $\mu\text{m}$ )	
Copper (0.5 OZ, 17.5 $\mu\text{m}$ )	BOT

## 2. Microstrips (TOP, BOT)

Substrate dielectric: 4.2

Substrate height: 120  $\mu\text{m}$

Trace thickness: 33  $\mu\text{m}$

Lower trace width – upper trace width = 25  $\mu\text{m}$

<b>Microstrip (RGMII)</b>	
Trace width ( $\mu\text{m}$ )	Impedance ( $\Omega$ )
150	59
200	51

<b>Differential Microstrip (XFI, LVDS)</b>		
Trace width ( $\mu\text{m}$ )	Separation ( $\mu\text{m}$ )	Impedance ( $\Omega$ )
150	150	100
180	270	100
190	360	100

## 3. Striplines (INTT, INTB)

Substrate dielectric: 4.2

Substrate height: 250 +200  $\mu\text{m}$

Trace thickness: 35  $\mu\text{m}$

Lower trace width – upper trace width = 25  $\mu\text{m}$

<b>Stripline (RGMII)</b>	
Trace width ( $\mu\text{m}$ )	Impedance ( $\Omega$ )
150	51
200	45