10 GB Communication & Control Card

Version 1.03

Instruction Manual

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Using this Document

This document is intended for the software and hardware engineer's reference and provides detailed information about the 10 GB Communication & Control Card. Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact ByteStudio (bytestudio@bytestudio.hu) for additional information that may help in the development process.

Document History

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1 Introduction

The 10 GB Communication and Control Card (10 GB C&C Card) controls timing of all ADC Boards in the system, collects data from the serial LVDS inputs, forms UDP packets and sends them to the DAQ PC on the 10 Gbit Ethernet XFP output line. Additionally it provides a parallel data interface (PDI) for programming both the ADC Boards and the APDCAM control card. Data to/from the parallel port is also transmitted in UDP packets to/from the DAQ PC.

2 Features

- Single 3.3 V power supply
- 10 GB Ethernet interface with XFP connector
- Separated 10Base-T and 100Base-TX management Ethernet interface with RJ45 connector
- 8 serial high-speed LVDS inputs
- 4 UDP Data Stream outputs
- On–board 256-Mbit SDRAM
- Easy to program via UDP/IP or HTTP
- Integrated WEB server (option)
- 8-bit instruction set (Digital Data Transmission over IP v3 – DDToIPv3)
- Protocols: ICMP ping, ARP, DHCP, UDP, TCP, HTTP
- Programmable ARP Report advertisement
- Status and overflow LED port
- Serial Communication Bus (SCB)
- Parallel Data Interface (PDI)
- External IO and Control ports
- Low power consumption, high reliability, long life time

3 Model List and Block Diagram

10 GB Communication and Control Card Model List:

Model	Features
10 GB C&C	10 GB Communication & Control Card Firmware group reference number: BSF12-0001 PCB reference number: BSP12-0001

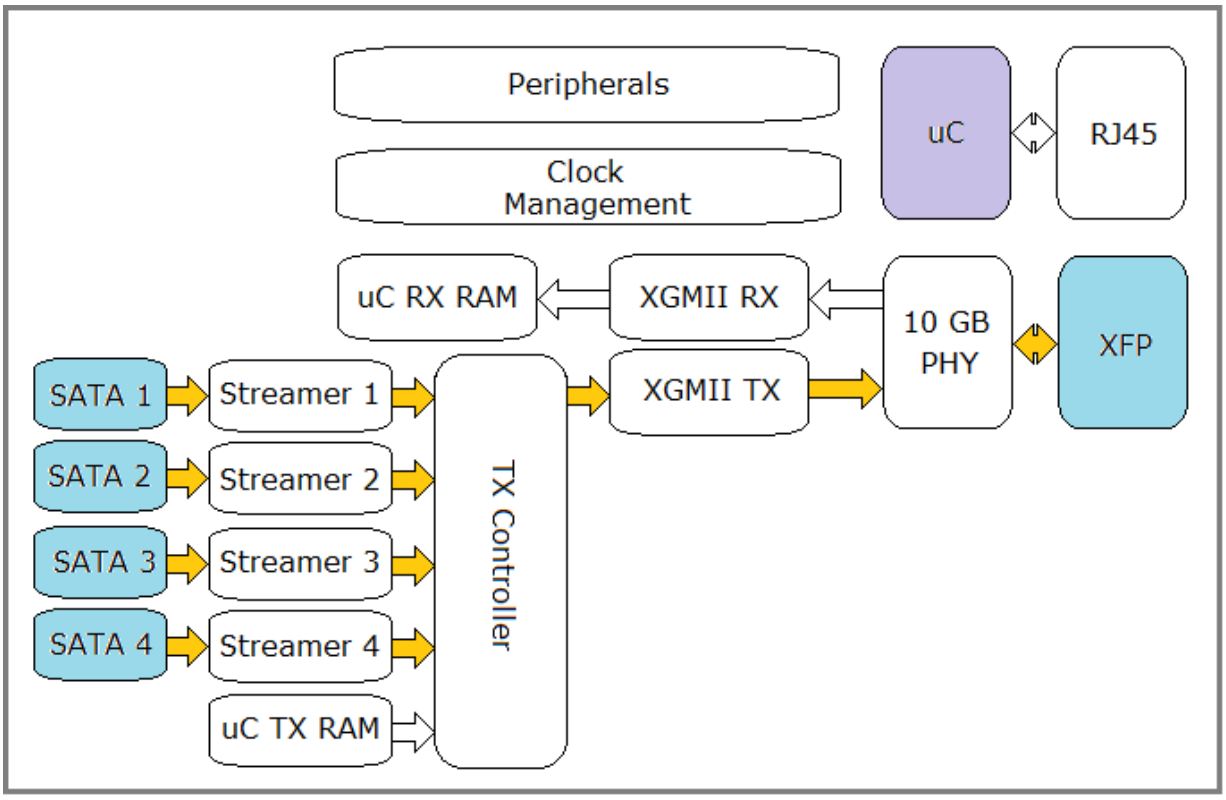
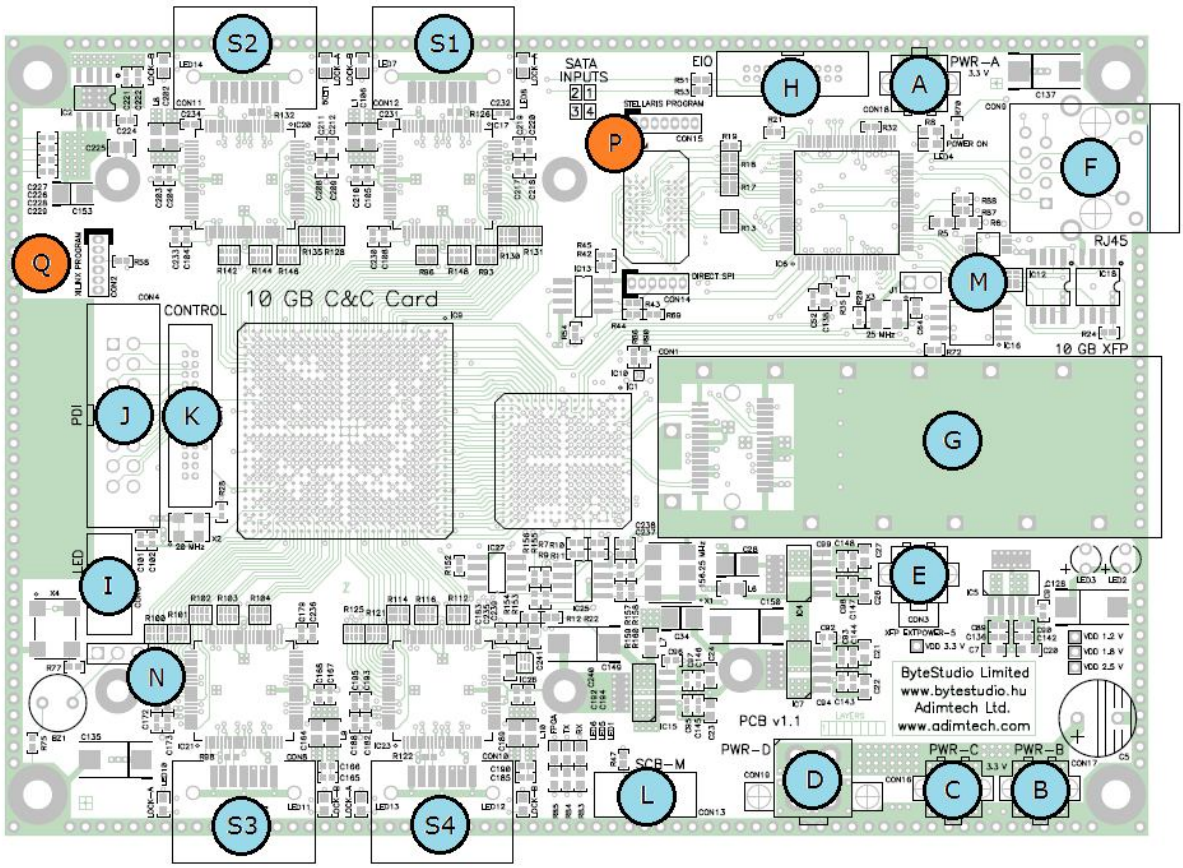


Figure 1. 10 GB Communication & Control Card Block Diagram

4 General Description



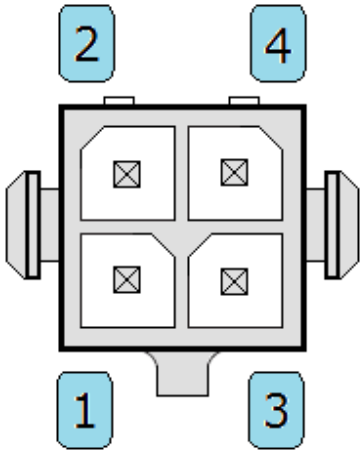
Char	Connector
A	PWR-A
B	PWR-B
C	PWR-C
D	PWR-D
E	XFP EXTPOWER-5
F	RJ45 ETHERNET INTERFACE (MANAGEMENT PORT)
G	10 GB XFP INTERFACE (STREAM PORT)
H	EIO
I	LED
J	PDI
K	CONTROL
L	SERIAL COMMUNICATION BUS RESET DEFAULTS SWITCH
M	J1 (RESET)

N	J2 (TEST)
P	Stellaris program (Don’t connect!)
Q	Xilinx program (Don’t connect!)
S1..4	SATA INPUTS

4.1 Power Supply

The 10 GB C&C Card needs single 3.3 V power supply. The board contains four main power connectors.

PWR-A, PWR-B and PWR-C (Connector A, B and C)
Connector Type: Tyco Micro MATE-N-LOK 3
(dual row, vertical, through hole mount)



Pin	Description	Direction
1	GND	
2	+3.3 V Power	Input
3	GND	
4	+3.3 V Power	Input

PWR-D (Connector D)
Connector Type: Tyco VAL-U-LOK
(2x2, vertical, through hole mount)

Pin	Description	Direction
1	GND	
2	+3.3 V Power	Input
3	GND	
4	+3.3 V Power	Input

The XFP module may require +5 V or -5 V power supply. The 5 V power can be connected to Connector E from an external source.

XFP EXTPOWER-5 (Connector E)
Connector Type: Tyco Micro MATE-N-LOK 3
(dual row, vertical, through hole mount)

Pin	Description	Direction
1	GND	
2	XFP -5 V Power	Input
3	GND	
4	XFP +5 V Power	Input

4.2 Device Management

Building the network and connecting the devices is made using the standard elements used in computer networks, no special elements or cables are required. For connecting a device UTP (Unshielded Twisted Pair) cables of at least category 5 have to be used. The connections are made with RJ45 8-pin telephony connectors (Connector F) or XFP modules (Connector G).

The management port complies with the 10Base-T and 100Base-TX IEEE 802.3 standards (UTP cable only). The Stream port contains a Marvell 88X2012 integrated 10 GB Ethernet transceiver that complies with the IEEE 802.3ae standard. The Marvell PHY provides all the necessary physical layer functions to over optical cable. The 10 GB C&C Card operates in full-duplex mode.

Using the management port the card can easily be programmed via UDP/IP or HTTP (TCP/IP). The device supports Digital Data Transmission over IP version 3 (DDToIPv3) protocol.

The 10 GB C&C Card supports several protocols that do not belong closely to the device management:

- ARP query and request (see RFC 826.)
- ICMP PING (see RFC 792)
- DHCP

DDToIPv1 compatibility: The device answers to SENDACK instruction.
DDToIPv2 compatibility: The device answers to SENDACK (General ACK Type) instruction.

4.2.1 IPv4 and MAC Addresses

The 10 GB C&C Card has programmable MAC addresses and programmable IPv4 addresses.

The MAC addresses can be set using the SETMAC instruction. The device supports three modes of setting the MAC address:

- In Factory Default mode the MAC Address is the factory default.
- In Static mode the user can freely set the MAC address.
- In CW Auto mode the device automatically computes the MAC address from its IP address (Figure 2). The first two bytes of the MAC address are constant 42:57 hexadecimal. The lower 4 bytes refer to the IPv4 address.

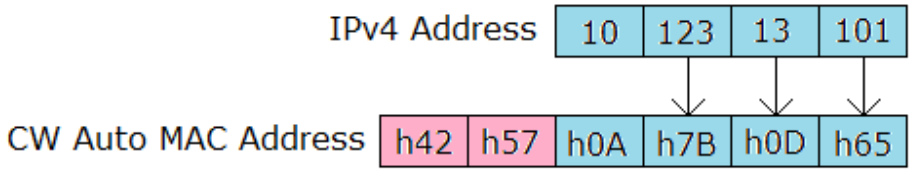


Figure 2. CW Auto MAC Mode

The IP addresses can be configured with the SETIPV4 instruction. Both Static IP and DHCP mode is supported. Note that the Internet Assigned Numbers Authority (IANA) has reserved the following three blocks of the IP address space for private networks (see RFC 1918):

Network Address Range	CIDR Notation
10.0.0.0 - 10.255.255.255	/8
172.16.0.0 - 172.31.255.255	/12
192.168.0.0 - 192.168.255.255	/16

Factory default settings (MAC addresses are given in hexadecimal format, IPv4 addresses in decimal format):

- Management port MAC address: 42:57:0A:7B:0D:65
- Management port IPv4 address: 10.123.13.101
- TS port MAC address: 42:57:0A:7B:0D:66
- TS port IPv4 address: 10.123.13.102
- Static IP and CW Auto MAC mode

4.2.2 Network Mask and Default Gateway

The network address space is usually organized into several subnets. Routers (default gateways) constitute borders between subnets. In IPv4, the subnet is identified by its base address and network mask.

The network mask can be programmed using the SETIPV4NETMASK instruction. The factory default value is 255.255.255.0. If the IP Mode is set to DHCP the controller automatically gets the network mask from the DHCP server.

A default gateway is a node (a router) on a network that serves as an access point to another network. The Default gateway can be programmed using the SETIPV4GATEWAY instruction. The device supports three gateway modes:

- None: There is no default gateway in the network.
- Static: The user sets the IP of the gateway. The gateway MAC address will be found by the device using ARP sequence.
- DHCP: The controller finds the default gateway with DHCP protocol.

References:

- RFC 950 Internet Standard Subnetting Procedure
- RFC 1812 New Internet Subnetting Procedure
- RFC 950 Utility of Subnets of Internet Networks
- RFC 1101 DNS Encodings of Network Names and Other Types

4.2.3 DDToIPv3 Protocol

Digital Data Transmission over IP Version 3 (DDToIPv3) is a flexible device management protocol originally developed for the Gigabit Ethernet Controller II. board. The instructions can be encapsulated in UDP/IP packets as shown in Figure 3 or in HTTP POST messages.

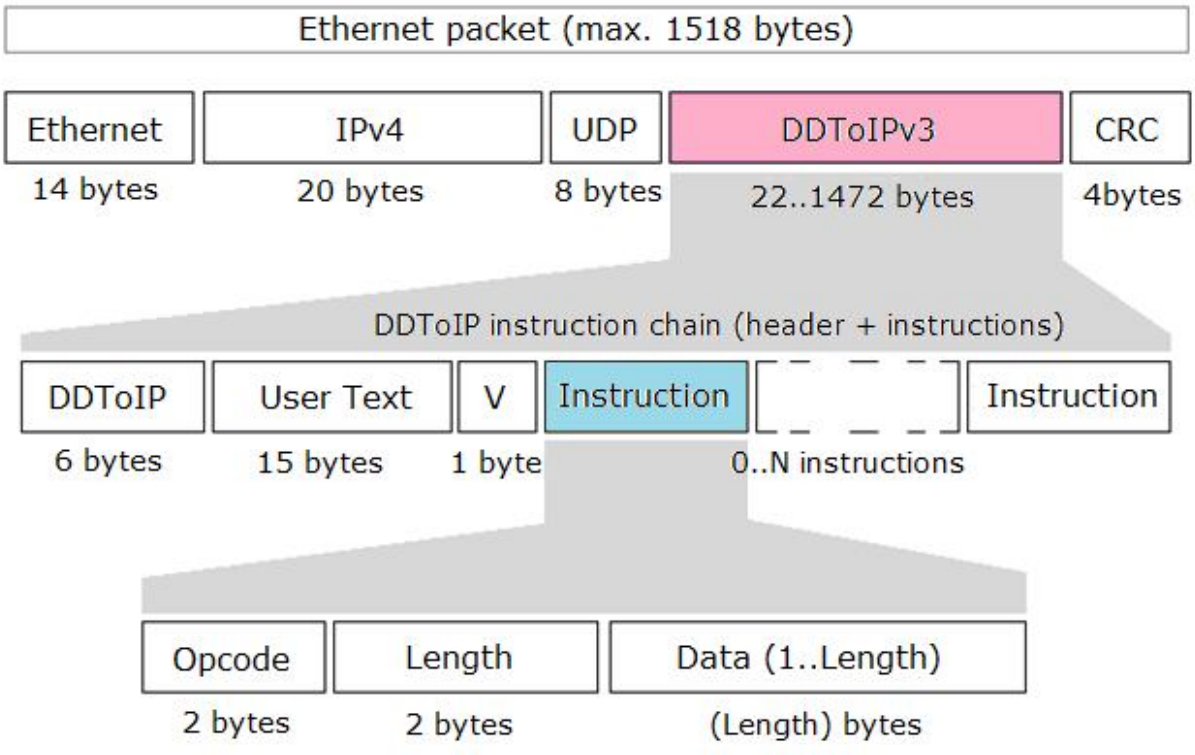


Figure 3. DDToIPv3 Protocol

The DDToIP instruction chain (contained by the UDP payload or the HTTP POST body) must start with "DDToIP" characters (44-44-54-6F-49-50 hexadecimal). It is followed by a 15-character user-defined string (User Text). User can use this field to place his company name into the packet. V (version number) must be 0x03.

The DDToIP packet can contain one or more instructions. The instructions are performed sequentially.

4.2.4 Device Management via HTTP

The 10 GB C&C Card can be programmed via TCP/IP using the HTTP GET and POST messages.

Using HTTP GET method the user can read data from the controller. The read instruction is coded in the URI string of the request line. Requests using GET only retrieve data and have no other effect.

URI	Instruction
SENDACKxx	Send ACK type xx (xx must be between 0 and 99)
READSDRAMppppp	Read a 1024-byte page from the SDRAM of the microcontroller (ppppp must be between 0 and 32767)
FLREADpppp	Read a 1024-byte page from the Storage Flash (pppp must be between 0 and 8191)
SCBREADCAaaaannnn	Read data from the communication area via the SCB. aaaa is the SCB Address in hexadecimal format (e.g. 01B0). nnnn is the number of bytes to read in decimal format.
STARTFUP	Calculate checksum, send FUP CHECKSUM answer and start firmware upgrade. (future release)

Request line examples:

- GET /SENDACK8 HTTP/1.1
- GET /READSDRAM0 HTTP/1.1
- GET /READSDRAM32456 HTTP/1.1
- GET /FLREAD29 HTTP/1.1

To program the card the user must send a HTTP POST message to the controller with the "POST /DDToIP HTTP…" request line. The body of the message contains the DDToIPv3 instruction chain (DDToIP header with the user text and the instructions). If the instruction chain contains read instructions (e.g. SENDACK, READSDRAM, FLREAD) the answer can read out sending a HTTP GET message with the "DDToIP" URI.

Request lines:

- POST /DDToIP HTTP/1.1
- GET /DDToIP HTTP/1.1

4.2.5 Integrated WEB Server

The Integrated Web Server is under development.

4.3 Clock management

The 10 GB C&C Card generates the ADC Clock (F4, 10-50 MHz), the Sample Clock (F6) and the DSLV Reference Clock (FD1, 15-66 MHz) signals. The ADC Clock and the Sample Clock are transmitted to the ADC boards through the Control connector in LVDS format.

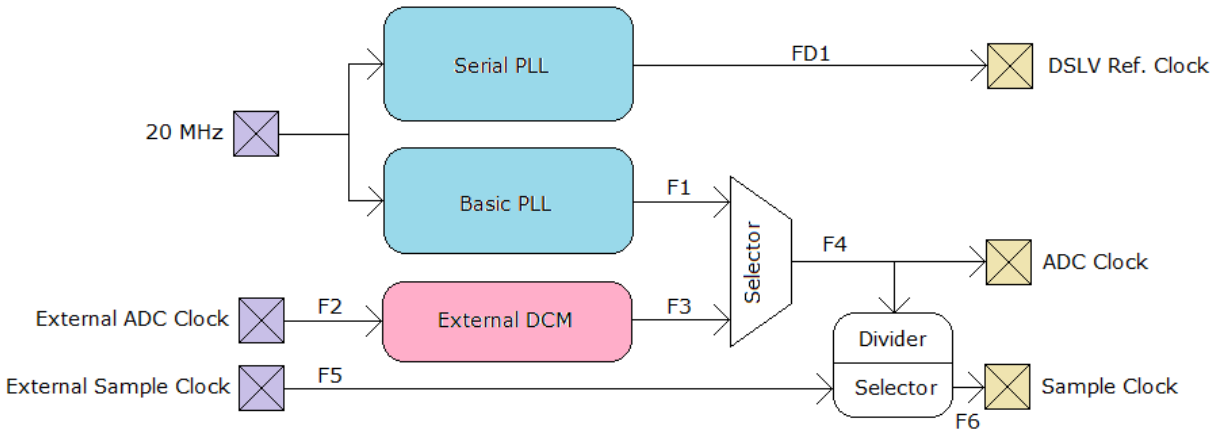


Figure 4. Clocking structure

The Serial PLL can be programmed using the PROGRAMSERIALPLL instruction. FD1 is generated from the internal 20 MHz crystal oscillator. The Serial PLL Multiply Value is 33 by default. (Note: FD1 and the DSLV clock frequency of the ADC Board must be met.)

$$FD1 = 20\ MHz \times \frac{Serial\ PLL\ Multiply\ Value\ (20..50)}{Serial\ PLL\ Divide\ Value\ 0\ (8..100)}$$

The Basic PLL can be programmed using the PROGRAMBASICPLL instruction. F1 and FD1 are generated from the internal 20 MHz crystal oscillator. The Basic PLL Multiply Value is 33 by default.

$$F1 = 20\ MHz \times \frac{Basic\ PLL\ Multiply\ Value\ (20..50)}{Basic\ PLL\ Divide\ Value\ 1\ (8..100)}$$

The lock status of the PLLs can be read out from the VARIABLES ACK (FPGA Status byte).

The ADC Clock (F4) can be generated from internal (F1) or external (F3) source. The Selector can be programmed by the SETCLOCKCONTROL instruction. When external clock signal is used the Selector has two different modes: normal and auto. In Auto External Clock Mode the Selector

automatically switches back to internal source if the external clock frequency (F2) is lower than 800 kHz or the External DCM is not locked.

F2 must be between 1 and 40 MHz. Use the PROGRAMEXTDCM instruction to configure the External DCM. The lock status of the DCM and the actual frequency of the external clock signal can be read out from the VARIABLES ACK (FPGA Status and External Clock Frequency).

$$F3 = F2 \times \frac{External\ DCM\ Multiply\ Value\ (2..33)}{External\ DCM\ Divide\ Value\ (1..32)}$$

The Sample Clock (F6) can be generated from the ADC Clock (F4) divided by a programmable value (Sample Divide Value) or from external source (F5). The Selector can be programmed by the SETCLOCKCONTROL instruction. Sample Divide Value should be greater than one.

The ADC Clock and the Sample Clock outputs of the CONTROL and the EIO connectors can be enabled and disabled using the SETCLOCKENABLE instruction.

4.4 UDP Streamer

The UDP Streamer collects data from the serial LVDS inputs (Connector S1..S4), forms UDP packets and sends them on the 10 Gbit Ethernet XFP output line. The card has four independent UDP Streamer modules. The input SATA connectors have 7 pins of which two pairs are used for fast LVDS connections. LVDS lines transmit two stream signals, the rest is ground. Standard computer SATA cable can be used to interconnect the ADC Board II. with the 10 GB C&C Card.

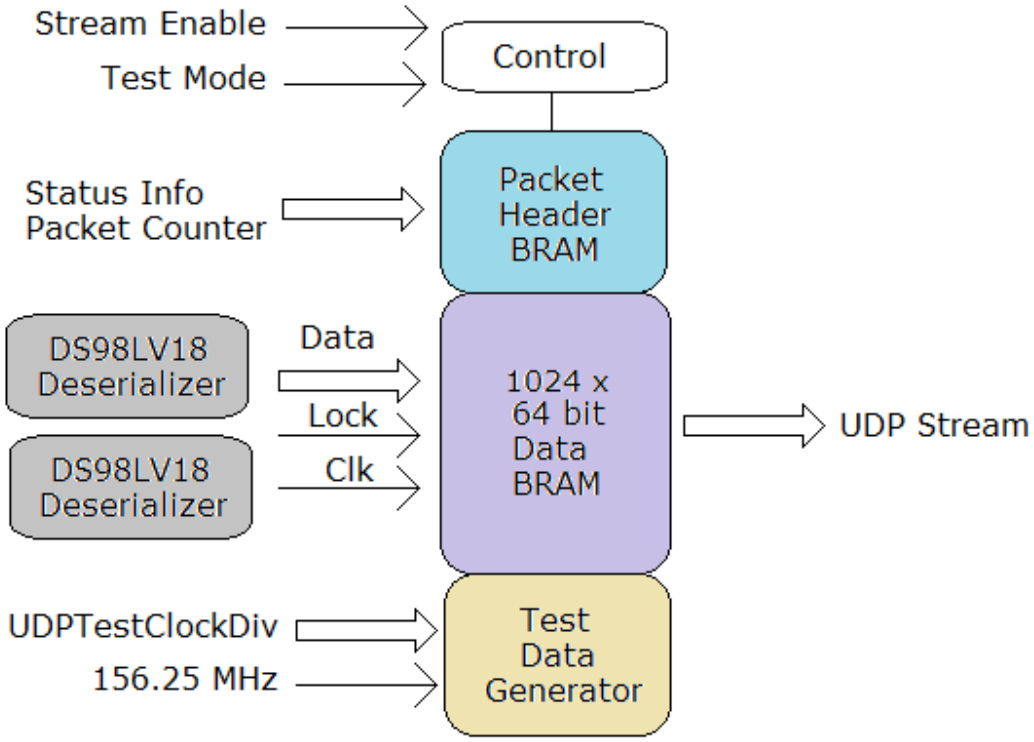


Figure 5. UDP Streamer

The IP stream properties (MAC Address, IP Address, UDP data length) can be set using the SETUDPSTREAM or the SETMULTICASTUDPSTREAM instructions. The streamer supports jumbo frames up to 8k data length. The UDP streams can be started or stopped using the SETSTREAMCONTROL instruction.

4.4.1 Packet format

The UDP packets contain C&C Header bytes and ADC data bytes. The UDP length of the packets are 22 + Octet * 8 bytes.

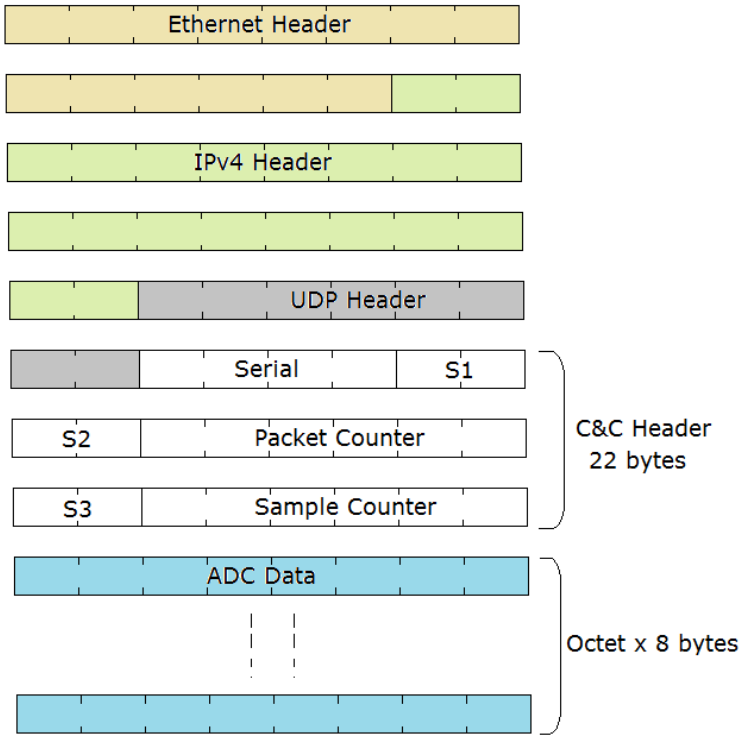


Figure 6. UDP Packet Structure

S1	
Bit	**Description**
15..14	Stream (00 – Stream1, …, 11 - Stream 4)
13..2	Reserved (0)
1	UDP Test Mode
0	Sample Start condition (The first data byte in the packet is the first byte of a sample.)

S2	
Bit	**Description**
15..8	FPGA Status (see VARIABLES ACK)
7..0	DSLV Lock Status

S3	
Bit	**Description**
15..8	Reserved (0)
7..0	Reserved (0)

4.4.2 UDP Test Mode

The UDP Test Mode can be switched on using the SETSREAMCONTROL instruction. In Test Mode the streamer periodically generates UDP test packets. The ADC Data field is filled with a test pattern. The delay between two UDP packets can be set using the SETUDPTESTCLOCKDIVIDER instruction.

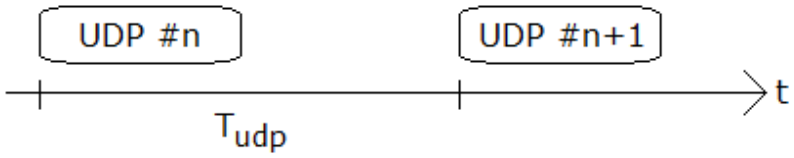


Figure 7. UDP Test Mode timing

T_{udp} = (UDP Test Clock Divider Value + 1) / 156250000 second

In Test Mode the sample counter is zero in the C&C header. The ADC data content of the test packets are the same. The first octet (first eight bytes) of the test pattern is h0001000100010001. This value is incremented by h0001000100010001 during the octets.

4.4.3 Stream start and stream stop conditions

The stream start condition depends on the trigger mode. Trigger options can be set using the SETTRIGGER instruction. The streamer unit has three different trigger modes:

- Non-triggered (Trigger sources are disabled, Trigger Control = 0x00)
- Triggered without delay (Trigger Control > 0, Trigger Delay = 0)
- Triggered with delay (Trigger Control > 0, Trigger Delay > 0)

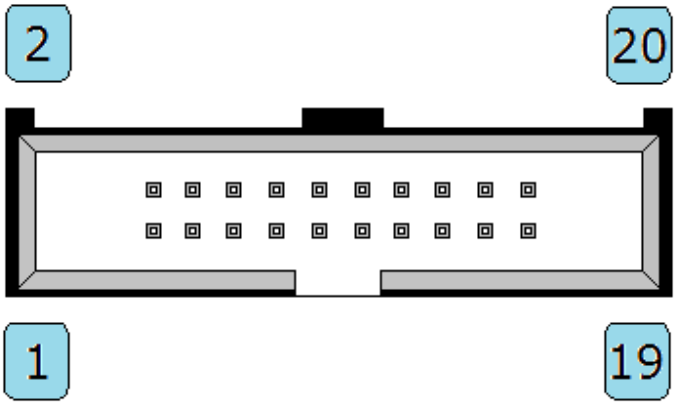
In non-triggered mode the streamer starts sending data immediately after the user set the Stream X enable/disable bit in the Stream Control register. In triggered mode the streamer waits for a trigger event after the user set the Stream X enable/disable bit in the Stream Control register. When a trigger event occurs it starts sending data (Trigger Delay = 0) or waits for Trigger Delay microseconds (except the user clears the Stream X enable/disable bit in the Stream Control register). Trigger events can be individually enabled or disabled with the SETTRIGGER instruction.

The stream stop condition depends on the Sample Count value. The Sample Count can be programmed using the SETSAMPLECOUNT instruction. The streamer unit has two different stream stop mode:

- Continuous: Sample Count = 0
- Counted: Sample Count > 0

In continuous mode the streamer stops sending data when the user clears the Stream X enable/disable bit in the Stream Control register. In counted mode the streamer counts the output samples and automatically stops sending data when the internal sample counter reaches the value set in the Sample Count.

4.5 EIO Connector

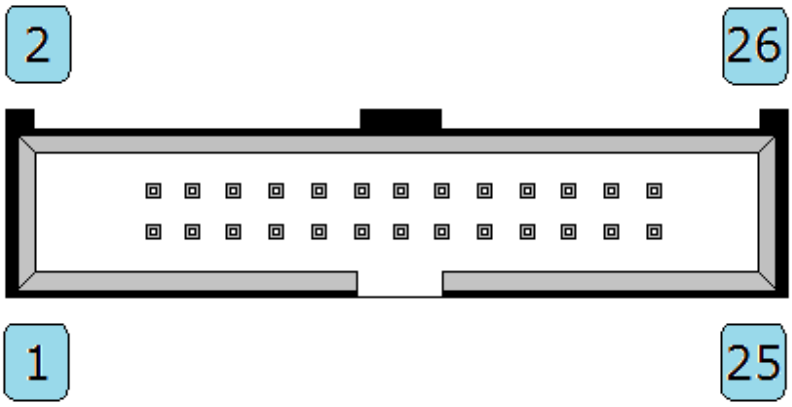


Connector type: Samtec SHF-110-01-L-D-TH
(Cable strip: Samtec FFSD-10-01-N)

Pin	Description	Direction	Impedance	IO Standard
1	GND			
2	EXT. TRIGGER IN	Input	4.7 kΩ pullup	3.3 V CMOS
3	TRIGGER OUT	Output		3.3 V CMOS
4	EXT. SAMPLE CLOCK	Input	4.7 kΩ pullup	3.3 V CMOS
5	SAMPLE CLOCK	Output		3.3 V CMOS
6	STREAMING	Output		3.3 V CMOS
7	FACTORY RESET	Input	4.7 kΩ pullup	3.3 V CMOS
8	ADC CLOCK	Output	27 Ω	3.3 V CMOS
9	GND			
10	EXT. ADC CLOCK	Input	4.7 kΩ pullup	3.3 V CMOS
11	GND			
12	SPARE IO 1	Output		3.3 V CMOS
13	SPARE IO 2	Output		3.3 V CMOS
14	SPARE IO 3	Output		3.3 V CMOS
15	SPARE IO 4	Output		3.3 V CMOS
16	TIMING 4	Output		3.3 V CMOS
17	TIMING 3	Output		3.3 V CMOS
18	TIMING 2	Output		3.3 V CMOS
19	TIMING 1	Output		3.3 V CMOS
20	GND			

4.6 Control Connector

The Control port (Connector CONTROL) is a 26-pin port on the board. The first 16 pins are used for the parallel port (PDI).



Connector type: Samtec SHF-113-01-L-D-TH
(Cable strip: Samtec FFSD-13-01-N)

Pin	Description	Direction	Impedance	IO Standard
1	DGND			
2	DATA 0	Bi-directional	2.2 kΩ pullup	3.3 V CMOS
3	DATA 1	Bi-directional	2.2 kΩ pullup	3.3 V CMOS
4	DATA 2	Bi-directional	2.2 kΩ pullup	3.3 V CMOS
5	DATA 3	Bi-directional	2.2 kΩ pullup	3.3 V CMOS
6	NC			
7	IRQ#	Input	2.2 kΩ pullup	3.3 V CMOS
8	DATA 4	Bi-directional	2.2 kΩ pullup	3.3 V CMOS
9	DATA 5	Bi-directional	2.2 kΩ pullup	3.3 V CMOS
10	DATA 6	Bi-directional	2.2 kΩ pullup	3.3 V CMOS
11	DATA 7	Bi-directional	2.2 kΩ pullup	3.3 V CMOS
12	WAIT#	Input	2.2 kΩ pullup	3.3 V CMOS
13	RESET#	Output		3.3 V CMOS
14	RW	Output		3.3 V CMOS
15	TE	Output		3.3 V CMOS
16	CLK	Output	27 Ω	3.3 V CMOS
17	INTERNAL TRIGGER	Input	Weak pullup	3.3 V CMOS

18	OVERLOAD	Input	Weak pullup	3.3 V CMOS
19	DATA OUT	Input	Weak pullup	3.3 V CMOS
20	DGND			
21	ADC CLOCK P	Output		LVDS
22	ADC CLOCK N	Output		LVDS
23	DGND			
24	SAMPLE CLOCK P	Output		LVDS
25	SAMPLE CLOCK N	Output		LVDS
26	DGND			

4.7 Parallel Data Interface

The 10 GB C&C Card has a two-way parallel port, through which data can directly be loaded from IP to the slave device or from the slave device to IP. Several slave devices can be connected to the bus. The Parallel Data Interface (PDI) has an 8-bit bi-directional data bus (DATA 0-7) and control signals: Clock (CLK), Transfer Enable (TE), Read/Write# (RW), IRQ#, WAIT# and RESET#.

Pin	Description	Direction	IO Standard	Impedance
1	GND	-	-	-
2	DATA 0	Bi-directional	3.3 V CMOS	2.2 kΩ pullup
3	DATA 1	Bi-directional	3.3 V CMOS	2.2 kΩ pullup
4	DATA 2	Bi-directional	3.3 V CMOS	2.2 kΩ pullup
5	DATA 3	Bi-directional	3.3 V CMOS	2.2 kΩ pullup
6	VDD (3.3 V)	-	-	-
7	IRQ#	Input	3.3 V CMOS	2.2 kΩ pullup
8	DATA 4	Bi-directional	3.3 V CMOS	2.2 kΩ pullup
9	DATA 5	Bi-directional	3.3 V CMOS	2.2 kΩ pullup
10	DATA 6	Bi-directional	3.3 V CMOS	2.2 kΩ pullup
11	DATA 7	Bi-directional	3.3 V CMOS	2.2 kΩ pullup
12	WAIT#	Input	3.3 V CMOS	2.2 kΩ pullup
13	RESET#	Output	3.3 V CMOS	2.2 kΩ pulldown
14	RW	Output	3.3 V CMOS	-
15	TE	Output	3.3 V CMOS	-
16	CLK	Output	3.3 V CMOS	27 Ω serial

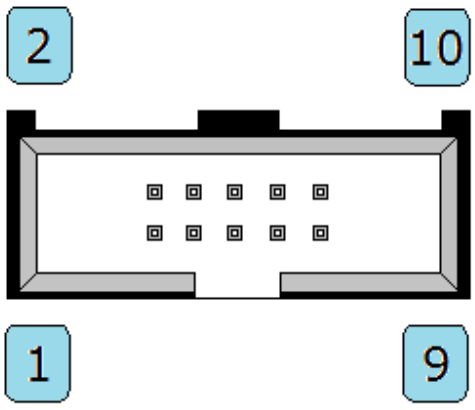
PDI data rate: 125 kB/s

A Read or a Write operation on the Parallel Data Interface can be performed using PDIREAD or PDIWRITE instructions. (Details about the PDI can be found in the GEC Instruction Manual Section 4.7)

4.8 LED Connector

The status LEDs port (connector I) is a 10-pin output port on the board and it can be used to directly drive the LEDs on the front panel of the device (serial resistors required). POWER ON is high after power up. ERROR is high if the Hardware Error register is not zero. The OVERLOAD output is driven by the OVERLOAD input of the CONTROL connector.

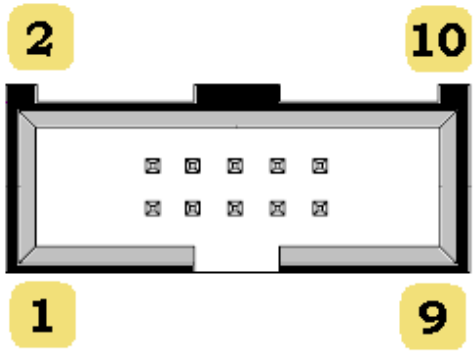
Pin	Description	Direction
1	GND	-
2	POWER ON	Output
3	ERROR	Output
4	STREAMING	Output
5	EXT. CLOCK VALID	Output
6	PDI COMMUNICATION	Output
7	OVERLOAD	Output
8	CAM TIMER ARMED	Output
9	CAM TIMER TRIGGER OUT	Output
10	GND	-



Connector type: Samtec SHF-105-01-L-D-TH
(Cable strip: Samtec FFSD-05-01-N)

4.9 Serial Communication Bus

The Serial Communication Bus (SCB-M) port (Connector L) is a 10-pin IO port on the board.



Connector type: Samtec SHF-105-01-L-D-TH
(Cable strip: Samtec FFSD-05-01-N)

Pin	Description	Direction	IO Standard	Impedance
1	GND	-	-	-
2	CLK	Output	3.3 V CMOS	27 Ω serial
3	GND	-	-	-
4	IRQ	Input	3.3 V CMOS	4.7 kΩ pulldown
5	GND	-	-	-
6	DI	Input	3.3 V CMOS	4.7 kΩ pulldown
7	GND	-	-	-
8	DO	Output	3.3 V CMOS	-
9	GND	-	-	-
10	RESET#	Output	3.3 V CMOS	4.7 kΩ pulldown

For more information about the SCB visit www.bytestudio.hu and download the latest user manual (Serial Communication Bus Vx.x) in pdf format.

4.10 CAM Timer

The CAM Timer unit is for generating 4-channel timing pulses on the EIO Connector. Timing pulses are produced by 10 identical timers, each capable of generating a sequence of pulses. Each timer has 4 individually adjustable parameters: delay time (32 bits) of the sequence, on-time 16 bits), off-time (16 bits) and number of pulses (28 bits). The Timer parameters can be programmed by the SETCTTIMER instruction.

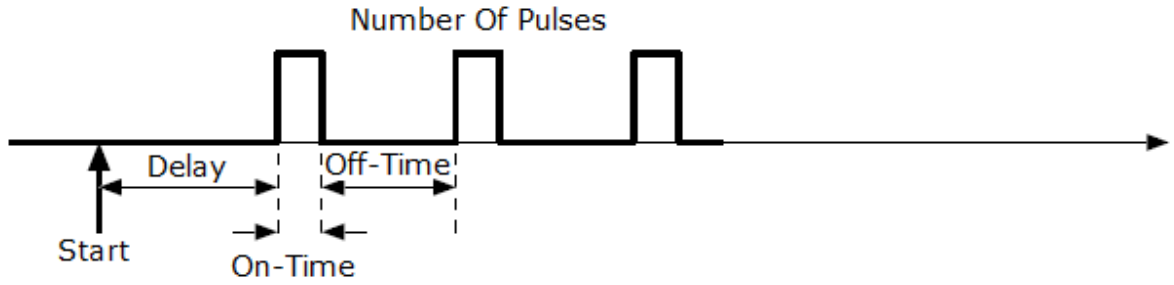


Figure 8. Timer parameters

The output of these timers can be combined to 4 output pulse sequences. Each timer can be OR connected to any of the four outputs and they can be enabled independently. The first 4 bits (bit 31 downto 28) of the 32-bit Number Of Pulses parameter in the SETCTTIMER instruction are the channel enable bits. The timing output parameters can be set by the SETCTOUTPUT instruction.

The reference clock signal of the timers is generated from the internal 20 MHz system clock divided by a programmable value (2 bytes giving a maximum division of 64K). This divided clock serves as the base clock for all the internal timers. The divider value can be programmed by the SETCTCLKDIV instruction.

The CAM Timer can be in one of three states: *idle*, *armed* or *running*. *Idle* is the default state after power-up, when the unit does not respond to trigger and does not produce output pulses. This state is normally used for setting up operation parameters. After programming is finished CAM Timer is set to *armed* state by setting bit 0 in the CAM Timer Control register. In this state the unit waits for trigger, still no timing pulses are generated. From *armed* state *running* state is entered on a trigger edge or when a start command is received (bit 1 of the CAM Timer Control register is set). Pulse generation starts from this time instance. Operation can be aborted by software command (clearing bit 0 or bit 1 in the CAM Timer Control register) or it ends when all 10 timers finished generating the requested number of pulses. Bits 2 and 3 in the CAM Timer Control register control the action to

be taken when all the timers finish pulse generation: CAM Timer immediately restarts operation with the previous settings (all internal counters will be reset), it enters to *armed* state and will wait for the next trigger event or it enters to *idle* state.

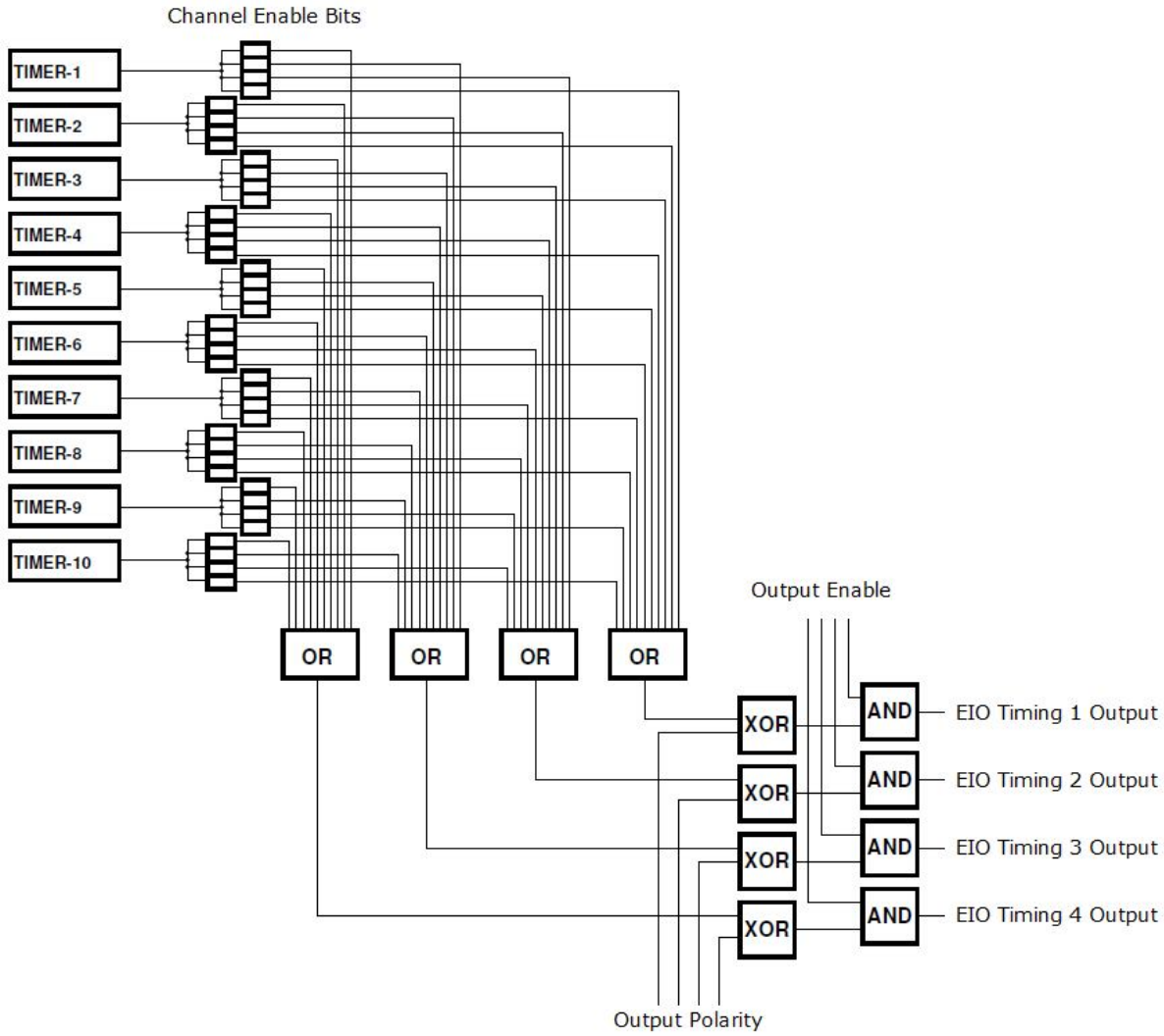


Figure 9. CAM Timer output generation

Three trigger events can be programmed: internal trigger, external trigger rising edge and external trigger falling edge.

4.11 Storage Flash

The 10 GB C&C Card has an optional on-chip 8-Mbyte SPI flash memory to store user data. The flash can be erased using the FLCHIPERASE, FLBLOCKERASE and FLBLOCKERASEW instructions. The flash can be programmed and read in 1024-byte pages using the FLPROGRAM and FLREAD instructions.

After performing an erase instruction (except FLBLOCKERASEW) the user must check the busy flag in the State register (see the Variables type ACK) to recognize the end of the erase process. While erase is being processed no other instructions can be performed by the flash memory.

4.12 Reset Defaults

The user can reset the default settings by shorting the Reset Defaults jumper. It is useful when the device is locked and user forgot the key, or the IP address of the device is unknown. To reset the default settings follow these steps:

- Switch on the device.
- Short the Reset Defaults jumper for a second.
- The controller sounds a blast, the device resets and starts working.

Settings changed to:

- Device Name:10 GB Communication & Control Card vX.XX
- Company Name: Adimtech Ltd.
- Host Name: BS-10GB-CC00
- User Text: Adimtech Ltd.
- Configuration word: 0x0000
- Management Port MAC Mode: CW-Auto
- Management Port IPv4 Address: 10.123.13.101
- Management Port Network Mask: 255.255.255.0
- Management Port IP Mode: Static
- Management Port Gateway Mode: None
- Management Port Gateway IPv4 Address: 10.123.13.1
- Management Port ARP Report Period: 15 sec
- Management Port IPv4 Time To Live: 128
- Stream Port MAC Mode: CW-Auto
- Stream Port IPv4 Address: 10.123.13.102
- Stream Port Network Mask: 255.255.255.0
- Stream Port IP Mode: Static
- Stream Port Gateway Mode: None
- Stream Port Gateway IPv4 Address: 10.123.13.1
- Stream Port ARP Report Period: 15 sec
- Stream Port IPv4 Time To Live: 128
- HTTP Port: 80

- Clock Control: 0x00
- Clock Enable: 0x0F
- Basic PLL Multiply Value: 33
- Basic PLL Divide 0 Value: 10
- Basic PLL Divide 1 Value: 33
- External DCM Multiply Value: 16

- External DCM Divide Value: 12
- Sample Divide Value: 10
- Spare IO: 0x00
- XFP: 0x01
- Sample Count: 0
- Trigger Control. 0x00
- Trigger Delay: 0

- Stream Control: 0x00
- UDP Test Clock Divider: 15624999
- Stream 1 Octet: 128
- Stream 1 IPv4 Address: 239.123.13.101
- Stream 1 UDP Port: 10001
- Stream 2 Octet: 128
- Stream 2 IPv4 Address: 239.123.13.102
- Stream 2 UDP Port: 10002
- Stream 3 Octet: 128
- Stream 3 IPv4 Address: 239.123.13.103
- Stream 3 UDP Port: 10003
- Stream 4 Octet: 128
- Stream 4 IPv4 Address: 239.123.13.104
- Stream 4 UDP Port: 10004

- CAM Timer Control: 0x0000

4.11 Self Test and Error Codes

After power on the 10 GB C&C Card performs a test sequence. If a critical error occurs the board cannot start up. In this case three status LEDs (the power on LED, the management port LINK LED and the ACT LED) are blinking. In case of non critical errors the corresponding flag in the Hardware Error register is set. The power on test sequence is the following:

1. Microcontroller SDRAM, EEPROM, External Flash1 and Flash2 test. SDRAM and EEPROM errors are critical. (In case of Flash1 error the WEB interface is not working, only the UDP based communication is active.)
2. Loading the settings from the EEPROM. An error is critical.
3. Waiting for FPGA program loading (boot). The card waits 2 seconds as a maximum. (In case of FPGA program error the management port of the controller is active, the user can read the Hardware Error register.)

In case of critical error the three status LEDs blink N times depends on the error type.

N	Error type	What to do?
2	SDRAM Error	Contact the vendor.
3	EEPROM Error	Power off and power on the device again or try to reset the default settings.
4	LOADSETTINGS error	Power off and power on the device again or try to reset the default settings.

5 Instruction Set

General instructions:

NOP	Opcode = 0x0000
LASTINSTRUCTION	Opcode = 0x0001
WAIT	Opcode = 0x0002
RESET	Opcode = 0x0003
LOCK	Opcode = 0x0004
UNLOCK	Opcode = 0x0005
SENDACK	Opcode = 0x0006
READSDRAM	Opcode = 0x0007

Configuration instructions:

SETSERIAL	Opcode = 0x0010
SETTYPE	Opcode = 0x0011
SETNAME	Opcode = 0x0012
SETUSERTEXT	Opcode = 0x0013
SETCOMPANY	Opcode = 0x0014
SETHOSTNAME	Opcode = 0x0015
SETCONFIGURATION	Opcode = 0x0016
IMPORTETTINGS	Opcode = 0x001E
SAVESETTINGS	Opcode = 0x001F

Network instructions:

SETMAC	Opcode = 0x0020
SETIPV4	Opcode = 0x0021
SETIPV4NETMASK	Opcode = 0x0022
SETIPV4GATEWAY	Opcode = 0x0023
SETARPREPORTPERIOD	Opcode = 0x0024
SETMACMODE	Opcode = 0x0025

Control instructions:

PROGRAMBASICPLL	Opcode = 0x0100
PROGRAMEXTDCM	Opcode = 0x0101
SETCLOCKCONTROL	Opcode = 0x0102
SETCLOCKENABLE	Opcode = 0x0103
PROGRAMSAMPLEDIVIDER	Opcode = 0x0104
SETSPAREIO	Opcode = 0x0105
SETXFP	Opcode = 0x0106
PROGRAMSERIALPLL	Opcode = 0x0107

Streamer instructions:

SETSTREAMCONTROL	Opcode = 0x0110
SETUDPTESTCLOCKDIVIDER	Opcode = 0x0111
SETMULTICASTUDPSTREAM	Opcode = 0x0112
SETUDPSTREAM	Opcode = 0x0113
SETSAMPLECOUNT	Opcode = 0x0114
SETTRIGGER	Opcode = 0x0115
CLEARTRIGGERSTATUS	Opcode = 0x0116
SETSATACONTROL	Opcode = 0x0117

CAM Timer instructions:

SETCTCONTROL	Opcode = 0x0120
SETCTOUTPUT	Opcode = 0x0121
SETCTCLKDIV	Opcode = 0x0122
SETCTTIMER	Opcode = 0x0123
SETCTIDLE	Opcode = 0x0124
SETCTARMED	Opcode = 0x0125
SETCTRUNNING	Opcode = 0x0126

SCB instructions:

SCBWRITECA	Opcode = 0x0060
SCBWRITERA	Opcode = 0x0061
SCBREADCA	Opcode = 0x0062
SCBREADRA	Opcode = 0x0063

PDI instructions:

PDIWRITE	Opcode = 0x0068
PDIREAD	Opcode = 0x0069

Storage Flash instructions:

FLCHIPERASE	Opcode = 0x0070
FLBLOCKERASE	Opcode = 0x0071
FLBLOCKERASEW	Opcode = 0x0072
FLPROGRAM	Opcode = 0x0073
FLREAD	Opcode = 0x0074

Firmware Upgrade and Test instructions

LOADFUP	Opcode = 0x0800
STARTFUP	Opcode = 0x0801
SHORTBEEP	Opcode = 0x0810

Answers:

ACKANSWER	Opcode = 0xFF00

SDRAMPAGE	Opcode = 0xFF01
SCBDATA	Opcode = 0xFF02
FLASHPAGE	Opcode = 0xFF03
PDIDATA	Opcode = 0xFF04

5.1 General Instructions

NOP instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0000					
3-4	Length							
5-	Data (optional)							

Description:

Do nothing.

LASTINSTRUCTION instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0001					
3-4	Length							
5-6	Data (optional)							

Description:

This is the last instruction is the chain. This instruction can be followed by any user data byte in the UDP packet.

WAIT instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0002					
3-4	Length		0x0002					
5-6	Wait							

Description:

Wait before processing the next instruction: $t_{Wait\ Time}$ = Wait [ms]

RESET instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0003					
3-4	Length		0x0003					
5	ResetType		0 – System Reset 1 - Serial Communication Bus Reset 2 – Parallel Data Interface Reset					
6-7	ResetTime							

Description:

The System Reset resets the whole controller. The reset time is about 2000 ms.

The ResetTime determines the width of the reset pulse during Serial Communication Bus Reset or Parallel Data Interface Reset:

$$t_{Reset\ Width} = \text{ResetTime [ms]}$$

LOCK instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0004					
3-4	Length		0x0010					
5-20	LockKey (MSB..LSB)							

Description:

The LOCK instruction locks the device with the LockKey. The locked device performs SENDACK, READSDRAM, FLREAD, SCBREADCA, SCBREADRA and UNLOCK instructions only. Don’t forget the LockKey! Without it you cannot unlock the device via Ethernet. If you forget the LockKey use the Reset Defaults pin to unlock the device.

UNLOCK instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0005					
3-4	Length		0x0010					
5-20	LockKey (MSB..LSB)							

Description:

Use the UNLOCK instruction to unlock a locked device. You must use the same LockKey, which was used to lock the device.

SENDACK instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0006					
3-4	Length		0x0002					
5-6	ACKType		0x0000 – DIT 0x0001 – Settings 0x0002 – DIT & Settings 0x0003 – Variables 0x0004 – Reserved 0x0801 – FUP Checksum					

Description:

Send an ACKANSWER message to the host computer (see section 5.10).

READSDRAM instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0007					
3-4	Length		0x0002					
5-6	Page Address							

Description:

Read the SDRAM memory of the microcontroller in 1024-byte pages. Page Address must be between 0 and 32767. Data read from the SDRAM is sent to the host computer encapsulated in a SDRAMPAGE answer message.

5.2 Configuration Instructions

SETSERIAL instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0010					
3-4	Length		0x0004					
5-8	Serial Number (MSB..LSB)							

Description:

Set the Serial Number. Serial Number is a user-defined 4-byte unsigned integer. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETTYPE instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0011					
3-4	Length		0x0002					
5-6	Type (MSB..LSB)							

Description:

Set the Type. Type is a user-defined 2-byte unsigned integer. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETNAME instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0012					
3-4	Length		0x0030					
5-52	Name (MSB..LSB)							

Description:

Set the Name. Name is a user-defined 48-byte (character) long string. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETUSERTEXT instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0013					
3-4	Length		0x000F					
5-19	User Text (MSB..LSB)							

Description:

Set the User Text. User Text is a user-defined 15-byte (character) long string in the DDToIP header (in device answers). (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETCOMPANY instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0014					
3-4	Length		0x0012					
5-22	Company (MSB..LSB)							

Description:

Set the Company. Company is a user-defined 18-byte (character) long string. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETHOSTNAME instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0015					
3-4	Length		0x000C					
5-16	Host Name (MSB..LSB)							

Description:

Set the Host Name. Host Name is a user-defined 12-byte (character) long string used in the DHCP messages. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETCONFIGURATION instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0016					
3-4	Length		0x0002					
5-6	Configuration (MSB..LSB)							

Description:

Set the Configuration. Configuration is a 2-byte unsigned integer. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

IMPORTSETTINGS instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x001E					
3-4	Length							
4-	Settings							

Description:

Import and save all the settings to the EEPROM.

SAVESETTINGS instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x001F					
3-4	Length		0x0000					

Description:

Save the settings to the EEPROM.

5.3 Network Instructions

SETMAC instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0020					
3-4	Length		0x0007					
5	P	0	0	0	0	0	MM	
6-11	MAC (MSB..LSB)							

Description:

Set and store the MAC address and mode. For details see section 4.2.1. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

P: 0 – Management port
1 – Stream port

MM: 0 – MAC mode is Factory Default
1 – MAC mode is CW-Auto
2 – MAC mode is Static

SETIPV4 instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0021					
3-4	Length		0x0005					
5	P	0	0	0	0	0	0	IM
6-9	IP (MSB..LSB)							

Description:

Set and store the IPv4 address and mode. For details see section 4.2.1. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

P: 0 – Management port
1 – Stream port

IM: 0 – IP mode is DHCP
1 – IP mode is Static

SETIPV4NETMASK instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0022					
3-4	Length		0x0005					
5	P	0	0	0	0	0	0	0
6-9	NetMask (MSB..LSB)							

Description:

Set and store the network mask. For details see section 4.2.2. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

P: 0 – Management port
1 – Stream port

Note: If the IP Mode is set to DHCP the controller automatically gets the network mask from the DHCP server.

SETIPV4GATEWAY instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0023					
3-4	Length		0x0005					
5	P	0	0	0	0	0	GM	
6-9	IP (MSB..LSB)							

Description:

Set and store the gateway parameters. For details see section 4.2.2. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

P: 0 – Management port
1 – Stream port

GM: 00 – Gateway mode is None
01 – Gateway mode is Static
10 – Gateway mode is DHCP

SETARPREPORTPERIOD instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0024					
3-4	Length		0x0002					
5	P	0	0	0	0	0	0	0
6	Report Period							

Description:

Set the ARP Auto-Report function. If the ARP Auto-Report function is on, the device periodically sends broadcast ARP reply messages ("the device is at its IP address"). If Report Period is set to zero (0x00) this function is switched off. Otherwise:

$$T_{ARP\ Report\ Period} = \text{Report Period [s]}$$

(Use the SAVESETTINGS instruction to save changes to the EEPROM.)

P: 0 – Management port
1 – Stream port

SETMACMODE instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0025					
3-4	Length		0x0001					
5	P	0	0	0	0	0	MM	

Description:

Set and store the MAC mode. For details see section 4.2.1. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

P: 0 – Management port
1 – Stream port

MM: 0 – MAC mode is Factory Default
1 – MAC mode is CW-Auto
2 – MAC mode is Static

5.4 Control Instructions

PROGRAMBASICPLL instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode 0x0100							
3-4	Length 0x0005							
5	Basic PLL Multiply Value							
6	Basic PLL Divide Value 0 (Reserved)							
7	Basic PLL Divide Value 1 (F1 Clock)							
8	Basic PLL Divide Value 2 (Reserved)							
9	Basic PLL Divide Value 3 (Reserved)							

Description:

Program the Basic PLL. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

PROGRAMEXTDCM instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode 0x0101							
3-4	Length 0x0002							
5	External DCM Multiply Value							
6	External DCM Divide Value							

Description:

Program the External DCM. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETCLOCKCONTROL instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0102					
3-4	Length		0x0001					
5	0	0	0	SS	AA	AS	0	0

Description:

Select ADC Clock and Sample source. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

AS: 0 – Internal AD Clock Source
1 – External AD Clock Source

AA: 0 – Normal External Clock Mode
1 – Auto External Clock Mode

AS: 0 – Internal Sample Source
1 – External Sample Source

SETCLOCKENABLE instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0103					
3-4	Length		0x0001					
5	0	0	0	0	ES	CS	EC	CC

Description:

Enable or disable clock outputs. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

ES: 0 – Disable sample output of the EIO connector
1 – Enable sample output of the EIO connector

CS: 0 – Disable sample output of the CONTROL connector
1 – Enable sample output of the CONTROL connector

EC: 0 – Disable clock output of the EIO connector
1 – Enable clock output of the EIO connector

CC: 0 – Disable clock output of the CONTROL connector
1 – Enable clock output of the CONTROL connector

PROGRAMSAMPLEDIVIDER instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0104					
3-4	Length		0x0002					
6-5	Sample Divide Value (MSB first)							

Description:

Program the Sample Clock divide value. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETSPAREIO instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0105					
3-4	Length		0x0001					
5	SpareIO							

Description:

Set the Spare IO port. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETXFP instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0106					
3-4	Length		0x0001					
5	0	0	0	0	0	0	0	CLK

Description:

Set the XFP port. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

CLK: 0 – Disable reference clock for the XFP module
1 – Enable reference clock for the XFP module

PROGRAMSERIALPLL instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode 0x0107							
3-4	Length 0x0005							
5	Serial PLL Multiply Value							
6	Serial PLL Divide Value 0 (DSLV Reference Clock)							
7	Reserved (0x00)							
8	Reserved (0x00)							
9	Reserved (0x00)							

Description:

Program the Serial PLL. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

5.5 Streamer Instructions

SETSTREAMCONTROL instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0110					
3-4	Length		0x0001					
5	TM4	TM3	TM2	TM1	EN4	EN3	EN2	EN1

Description:

Enable or disable the UDP streams. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

EN1: 0/1 – Stream 1 disabled/enabled
EN2: 0/1 – Stream 2 disabled/enabled
EN3: 0/1 – Stream 3 disabled/enabled
EN4: 0/1 – Stream 4 disabled/enabled
TM1: 0/1 – Testmode of Stream 1 disabled/enabled
TM2: 0/1 – Testmode of Stream 2 disabled/enabled
TM3: 0/1 – Testmode of Stream 3 disabled/enabled
TM4: 0/1 – Testmode of Stream 4 disabled/enabled

SETUDPTESTCLOCKDIVIDER instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0111					
3-4	Length		0x0004					
5-8	UDP Test Clock Divider Value (MSB..LSB)							

Description:

Set the UDP Test Clock Divider value. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETMULTICASTUDPSTREAM instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode 0x0112							
3-4	Length 0x0009							
5	Stream Number (1..4)							
6-7	Octet (MSB..LSB)							
8-11	IPv4 Multicast Address (MSB..LSB)							
12-13	UDP Port (MSB..LSB)							

Description:

Configure a multicast UDP stream. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

(UDP data size = 22 + Octet * 8)

SETUDPSTREAM instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode 0x0113							
3-4	Length 0x000F							
5	Stream Number (1..4)							
6-7	Octet (MSB..LSB)							
8-13	MAC Address (MSB..LSB)							
14-17	IPv4 Multicast Address (MSB..LSB)							
18-19	UDP Port (MSB..LSB)							

Description:

Configure an UDP stream. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETSAMPLECOUNT instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0114					
3-4	Length		0x0006					
5-10	Sample Count (MSB..LSB)							

Description:

Set the Sample Count. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETTRIGGER instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0115					
3-4	Length		0x0005					
5	0	DT	0	0	0	IT	ETF	ETR
6-9	Trigger Delay (MSB..LSB)							

Description:

Set the Trigger Control and the Trigger Delay (in us) values. The SETTRIGGER instruction clears the Trigger Status. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

ETR: 0/1 – External trigger rising slope disabled/enabled
ETF: 0/1 – External trigger falling slope disabled/enabled
IT: 0/1 – Internal trigger disabled/enabled
DT: Disable trigger event if streams are disabled (1)

CLEARTRIGGERSTATUS instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0116					
3-4	Length		0x0000					

Description:

Clear the Trigger Status.

SETSATACONTROL instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0117					
3-4	Length		0x0001					
5	0	0	0	0	0	0	0	DSM

Description:

Set the SATA Control register. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

DSM: 0/1 – Dual SATA Mode disabled/enabled

5.6 CAM Timer Instructions

SETCTCONTROL instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0120					
3-4	Length		0x0002					
5	0	0	0	0	0	0	0	0
6	0	IT	ETF	ETR	Mode		S	A

Description:

Set the control register of the CAM Timer module. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

A: 0/1 – Idle/Armed state

S: 0/1 – Manual Stop/Start

Mode: 00 – Return to Idle state after all the timers finish pulse generation.

01 – Return to Armed state after all the timers finish pulse generation.

10 – Return to Running state after all the timers finish pulse generation.

ETR: 0/1 – External trigger rising slope disabled/enabled

ETF: 0/1 – External trigger falling slope disabled/enabled

IT: 0/1 – Internal trigger disabled/enabled

SETCTOUTPUT instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0121					
3-4	Length		0x0002					
5	Output Polarity				Output Enabled			
6	Output in Armed state				Output in Idle state			

Description:

Set the output register of the CAM Timer module. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETCTCLKDIV instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0122					
3-4	Length		0x0002					
5-6	Clock Divide Value (MSB..LSB)							

Description:

Set the Clock Divide Value of the CAM Timer module. Divide value must be greater than 1. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

SETCTTIMER instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0123					
3-4	Length		0x000D					
5	Timer (1..10)							
6-9	Delay (MSB..LSB)							
10-11	On (MSB..LSB)							
12-13	Off (MSB..LSB)							
14-17	Number of Pulses (MSB..LSB)							

Description:

Set the timer parameters of the CAM Timer module. (Use the SAVESETTINGS instruction to save changes to the EEPROM.)

Note: The first 4 bits (bit 31..28) of the 32-bit Number Of Pulses parameter are the channel enable bits.

SETCTIDLE instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0124					
3-4	Length		0x0000					

Set the CAM Timer into Idle state. (Bit 1 and bit 0 of the control register are cleared.)

SETCTARMED instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0125					
3-4	Length		0x0000					

Set the CAM Timer into Armed state. (Bit 1 of the control register is cleared and bit 0 of the control register is set.)

SETCTRUNNING instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0126					
3-4	Length		0x0000					

Set the CAM Timer into Running state. (Bit 1 of the control register is set.)

5.7 SCB Instructions

SCBWRITECA instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode 0x0060							
3-4	Length							
5-6	SCB Address (MSB..LSB)							
7-	Data							

Description:

Write to the SCB Communication Area. SCB Address can be a unique or a broadcast (0xnnnF) address.

SCBWRITERA instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode 0x0061							
3-4	Length							
5-6	SCB Address (MSB..LSB)							
7-8	Register Address (MSB..LSB)							
9-	Data							

Description:

Write to the SCB Register Area. SCB Address can be a unique or a broadcast (0xnnnF) address. Register Address must be between 0 and 511.

SCBREADCA instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0062					
3-4	Length		0x0004					
5-6	SCB Address (MSB..LSB)							
7-8	Number Of Bytes (MSB..LSB)							

Description:

Read from to the SCB Communication Area. SCB Address must be a unique address. Data is sent to the host computer encapsulated in a SCBDATA answer message.

SCBREADRA instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0063					
3-4	Length		0x0006					
5-6	SCB Address (MSB..LSB)							
7-8	Register Address (MSB..LSB)							
9-10	Number Of Bytes (MSB..LSB)							

Description:

Read from the SCB Register Area. SCB Address must be a unique address. Register Address must be between 0 and 511. Data is sent to the host computer encapsulated in a SCBDATA answer message.

5.8 PDI Instructions

PDIWRITE instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0068					
3-4	Length							
5	Address							
6-9	SubAddress (MSB..LSB)							
10-	Data							

Description:

Write the data bytes to the selected Address and SubAddress through the Parallel Data Interface.

PDIREAD instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0069					
3-4	Length		0x0007					
5	Address							
6-9	SubAddress (MSB..LSB)							
10-11	NOB (MSB..LSB)							

Description:

Read NOB (number of data bytes) data bytes from the selected Address and SubAddress through the Parallel Data Interface. Data read from the slave device is sent to the host computer encapsulated in a PDIDATA answer message.

5.9 Storage Flash Instructions

FLCHIPERASE instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0070					
3-4	Length		0x0000					

Description:

Full chip erase of the 8-Mbyte storage flash. The instruction sets all memory to the erased state of all 1s (hFF). The busy flag (bit 1 in the State register of the Variables) is 1 during the erase and becomes 0 when finished and the device is ready to accept other instructions again. User must check this flag by receiving Variables type ACKs. The maximum of the chip erase time is 30 seconds (typ. 15 sec.).

FLBLOCKERASE instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0071					
3-4	Length		0x0001					
5	Block							

Description:

The instruction sets all memory within the specified block (64-Kbytes) to the erased state of all 1s (hFF). The busy flag (bit 1 in the State register of the Variables) is 1 during the erase and becomes 0 when finished and the device is ready to accept other instructions again. User must check this flag by receiving Variables type ACKs. The maximum of the block erase time is 1 second (typ. 150 ms).

FLBLOCKERASEW instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0072					
3-4	Length		0x0001					
5	Block							

Description:

The instruction sets all memory within the specified block (64-Kbytes) to the erased state of all 1s (hFF). The controller waits while the busy flag (bit 1 in the State register of the Variables) becomes 0. The maximum of the block erase time is 1 second (typ. 150 ms).

FLPROGRAM instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0073					
3-4	Length							
5-7	Address (MSB..LSB)							
8-	Data							

Description:

The instruction allows 1 to 1024 bytes of data to be programmed at previously erased (hFF) memory locations. Address must be between 0 and 8388607 (0x7FFFFF). Typical program time of 1024 bytes is 700 us.

FLREAD instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0074					
3-4	Length		0x0002					
5-6	Page Address (MSB..LSB)							

Description:

Read the flash memory in 1024-byte pages. Page Address must be between 0 and 8191. Data read from the flash memory is sent to the host computer encapsulated in a FLASHPAGE answer message.

5.10 Firmware Upgrade and Test Instructions

LOADFUP instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0800					
3-4	Length		L					
5-8	Address		0x00000000 – 0x00800000					
9-	Data							

Description:

Not public.

STARTFUP instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0801					
3-4	Length		0x0004					
5-8	Upgrade Date (4 bytes long date field, the format is Y[2]M[1]D[1].)							

Description:

Not public.

SHORTBEEP instruction

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0x0810					
3-4	Length		L					
5-	Optional stuffing bytes							

Description:

The controller sounds a blast. This instruction is used for test.

5.11 Answers

ACKANSWER message

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0xFF00					
3-4	Length		L					
5-6	Type							
7-	ACK Data							

Description:

This is the answer for the SENDACK instruction. The ACK Data can be the following depending on the Type field:

- 0x0000 – DIT
- 0x0001 – Settings
- 0x0002 – DIT & Settings
- 0x0003 – Variables
- 0x0004 – Reserved
- 0x0801 – FUP Checksum

DIT

Every device developed by ByteStudio Limited has a Device Identity Table (DIT, 64 bytes) which stores the main read-only manufacturing properties. All fields are MSB first.

Byte	7	6	5	4	3	2	1	0
7-16	Board Type (10 bytes long string = "BSP12-0001".)							
17-30	Firmware Group (14 bytes long string = "BSF12-0001-xxx", where xxx is the version number (e.g. 101 = version 1.01).)							
31-32	Firmware Group Version (2 bytes long version, the format is VH[1].VL[1] (the first is the version high, the second is the version low).)							
33-36	Upgrade Date (4 bytes long date field, the format is Y[2]M[1]D[1].)							
37-50	Manufacturer Firmware Group (14 bytes long firmware group programmed originally by the manufacturer.)							
51-54	Manufacturer Program Date (4 bytes long date of the manufacturer programming.)							
55-58	Manufacturer Serial (4 bytes long unique serial number.)							

59-62	Manufacturer Test Result (4 bytes long test result.)
63-70	Reserved (8 bytes long reserved field.)

SETTINGS

Settings are the writable registers of the device. The settings can be set using the configuration, network, control and streamer instructions.

Byte	7	6	5	4	3	2	1	0
7	Settings Version (version number of the data structure, for internal use)							
8-55	Device Name (48 bytes long string, e.g. "10 GB Communication and Control Card v1.00".)							
56-57	Device Type (2 bytes long integer, MSB first.)							
58-61	Device Serial (4 bytes long integer, MSB first.)							
62-79	Company Name (18 bytes long string, e.g. "ByteStudio Limited".)							
80-91	Host Name (12 bytes long string, used in the DHCP messages.)							
92-93	Configuration (2 bytes long configuration word, MSB first.) Bit 0 – Device is locked (1) / unlocked (0) Bit 1..15 – Reserved (0)							
94-108	User Text (15 bytes long string, used in the DDToIP header.)							
109-110	Reserved (0x0000)							
111-112	Reserved (0x0000)							
113-114	Reserved (0x0000)							
115-116	Reserved (0x0000)							
117-118	Reserved (0x0000)							
119-120	Reserved (0x0000)							

121-134	Reserved (0x00)
135-140	Management Port Static MAC Address (MSB first)
141-144	Management Port IPv4 Address (MSB first)
145-148	Management Port IPv4 Network Mask (MSB first)
149	Management Port MAC Mode (0 – Factory Default, 1 – CW-Auto, 2 – Static)
150	Management Port IP Mode (1 – Static , 2 - DHCP)
151	Management Port Gateway Mode (0 – None, 1 – Static , 2 - DHCP)
152-155	Management Port Gateway IPv4 Address (MSB first)
156	Management Port ARP Advertisement Report Period (in second, 0 = this function is off)
157	Management Port IGMP Report Period (in second, 0 = this function is off)
158	Management Port IPv4 Time To Live (TTL value in the IPv4 header)
159-164	Management Port Factory Default MAC Address (MSB first)
165-182	Reserved (0x00)
183-188	Stream Port Static MAC Address (MSB first)
189-192	Stream Port IPv4 Address (MSB first)
193-196	Stream Port IPv4 Network Mask (MSB first)
197	Stream Port MAC Mode (0 – Factory Default, 1 – CW-Auto, 2 – Static)
198	Stream Port IP Mode (1 – Static , 2 - DHCP)
199	Stream Port Gateway Mode (0 – None, 1 – Static , 2 - DHCP)
200-203	Stream Port Gateway IPv4 Address (MSB first)
204	Stream Port ARP Advertisement Report Period (in second, 0 = this function is off)
205	Stream Port IGMP Report Period (in second, 0 = this function is off)
206	Stream Port IPv4 Time To Live (TTL value in the IPv4 header)
207-212	Stream Port Factory Default MAC Address (MSB first)

213-230	Reserved (0x00)
231-232	HTTP Port (LSB first!)
233-234	SMTP Server Port (LSB first!)
235-262	Reserved (0x00)
263	Clock Control (See the SETCLOCKCONTROL instruction.)
264	Clock Enable (See the SETCLOCKENABLE instruction.)
265	Basic PLL Multiply Value
266	Basic PLL Divide Value 0
267	Basic PLL Divide Value 1
268	Basic PLL Divide Value 2
269	Basic PLL Divide Value 3
270	External DCM Multiply Value
271	External DCM Divide Value
272-273	Sample Divide Value (MSB first)
274	Spare IO Bit 0..3 : Spare IO bits Bit 7..4 : Reserved
275	XFP Bit 0 : XFP Reference Clock Enable Bit 7..1 : Reserved
276-281	Sample Count (MSB first)
282	Trigger Control (See the SETTRIGGER instruction.)
283-286	Trigger Delay (MSB First)
287	Serial PLL Multiply Value
288	Serial PLL Divide Value 0
289-291	Reserved (0x00)
292	SATA Control
293-298	Reserved (0x00)
299	Stream Control (See the SETSTREAMCONTROL instruction.)
300-303	UDP Test Clock Divider Value (MSB first)
304-	Reserved (0x00)

310	
311-312	Stream 1 Octet (MSB first)
313-318	Stream 1 MAC Address (MSB first)
319-322	Stream 1 IPv4 Address (MSB first)
323-324	Stream 1 UDP Port (MSB first)
325-326	Reserved (0x00)
327-328	Stream 2 Octet (MSB first)
329-334	Stream 2 MAC Address (MSB first)
335-338	Stream 2 IPv4 Address (MSB first)
339-340	Stream 2 UDP Port (MSB first)
341-342	Reserved (0x00)
343-344	Stream 3 Octet (MSB first)
345-350	Stream 3 MAC Address (MSB first)
351-354	Stream 3 IPv4 Address (MSB first)
355-356	Stream 3 UDP Port (MSB first)
357-358	Reserved (0x00)
359-360	Stream 4 Octet (MSB first)
361-366	Stream 4 MAC Address (MSB first)
367-370	Stream 4 IPv4 Address (MSB first)
371-372	Stream 4 UDP Port (MSB first)
273-274	Reserved (0x00)

275-278	CT Timer 1 Delay (MSB first)
279-280	CT Timer 1 On (MSB first)
281-282	CT Timer 1 Off (MSB first)
283-286	CT Timer 1 Number of Pulses (MSB first)
287-290	CT Timer 2 Delay (MSB first)
291-292	CT Timer 2 On (MSB first)
293-294	CT Timer 2 Off (MSB first)
295-298	CT Timer 2 Number of Pulses (MSB first)
299-302	CT Timer 3 Delay (MSB first)
303-304	CT Timer 3 On (MSB first)
305-306	CT Timer 3 Off (MSB first)
309-310	CT Timer 3 Number of Pulses (MSB first)
311-314	CT Timer 4 Delay (MSB first)
315-316	CT Timer 4 On (MSB first)
317-318	CT Timer 4 Off (MSB first)
319-322	CT Timer 4 Number of Pulses (MSB first)
323-326	CT Timer 5 Delay (MSB first)
327-328	CT Timer 5 On (MSB first)
329-330	CT Timer 5 Off (MSB first)
331-334	CT Timer 5 Number of Pulses (MSB first)
335-	CT Timer 6 Delay (MSB first)

338	
339-340	CT Timer 6 On (MSB first)
341-342	CT Timer 6 Off (MSB first)
343-346	CT Timer 6 Number of Pulses (MSB first)
347-350	CT Timer 7 Delay (MSB first)
351-352	CT Timer 7 On (MSB first)
353-354	CT Timer 7 Off (MSB first)
355-358	CT Timer 7 Number of Pulses (MSB first)
359-362	CT Timer 8 Delay (MSB first)
363-364	CT Timer 8 On (MSB first)
365-366	CT Timer 8 Off (MSB first)
367-370	CT Timer 8 Number of Pulses (MSB first)
371-374	CT Timer 9 Delay (MSB first)
375-376	CT Timer 9 On (MSB first)
377-378	CT Timer 9 Off (MSB first)
379-382	CT Timer 9 Number of Pulses (MSB first)
383-386	CT Timer 10 Delay (MSB first)
387-388	CT Timer 10 On (MSB first)
389-390	CT Timer 10 Off (MSB first)
391-394	CT Timer 10 Number of Pulses (MSB first)
395-396	CAM Timer Control (MSB first)

397-398	CAM Timer Clock Divide Value (MSB first)
399-400	CAM Timer Output (MSB first)
401-402	Reserved (0x0000)

DIT & SETTINGS

Byte	7	6	5	4	3	2	1	0
7-70	DIT							
71-	Settings							

VARIABLES

Variables are the read-only registers of the device. The variables cannot be set.

Byte	7	6	5	4	3	2	1	0
7-12	Management Port MAC Address (MSB first)							
13-16	Management Port IPv4 Address (MSB first)							
17-20	Management Port IPv4 Network Mask (MSB first)							
21	Management Port Link On (0 = Link is off, 1 = Link is on)							
22	Management Port Gateway State (0 = None, 1 = OK, 2 = Searching MAC, 3 = Searching IP with DHCP)							
23	Management Port IP State (1 = OK, 3 = Searching IP with DHCP)							
24	Management Port DHCP State (0 = Idle, 1 = Request, 2 = Discover)							
25-30	Management Port Gateway MAC Address (MSB first)							
31-34	Management Port Gateway IPv4 Address (MSB first)							
35-40	Management Port DHCP Server MAC Address (MSB first)							

41-44	Management Port DHCP Server IPv4 Address (MSB first)
45-50	Management Port IGMP Switch MAC Address (MSB first)
51-54	Management Port IGMP Switch IPv4 Address (MSB first)
55-58	Management Port DHCP Lease Time (LSB first!)
59-62	Management Port Ethernet RX Frames (LSB first!)
63-66	Management Port Ethernet TX Frames (LSB first!)
67-70	Reserved (0x00)
71-76	Stream Port MAC Address (MSB first)
77-80	Stream Port IPv4 Address (MSB first)
81-84	Stream Port IPv4 Network Mask (MSB first)
85	Stream Port Link On (0 = Link is off, 1 = Link is on)
86	Stream Port Gateway State (0 = None, 1 = OK, 2 = Searching MAC, 3 = Searching IP with DHCP)
87	Stream Port IP State (1 = OK, 3 = Searching IP with DHCP)
88	Stream Port DHCP State (0 = Idle, 1 = Request, 2 = Discover)
89-94	Stream Port Gateway MAC Address (MSB first)
95-98	Stream Port Gateway IPv4 Address (MSB first)
99-104	Stream Port DHCP Server MAC Address (MSB first)
105-108	Stream Port DHCP Server IPv4 Address (MSB first)
109-114	Stream Port IGMP Switch MAC Address (MSB first)
115-118	Stream Port IGMP Switch IPv4 Address (MSB first)

119-122	Stream Port DHCP Lease Time (LSB first!)
123-126	Stream Port Ethernet RX Frames (LSB first!)
127-130	Stream Port Ethernet TX Frames (LSB first!)
131-134	Reserved (0x00)
135	Management Port Ethernet Buffers Used
136	Management Port Ethernet Buffers Used Max.
137-138	Reserved (0x00)
139-142	Management Port Ethernet Dropped Frames (LSB first!)
143-146	Management Port TCP RX Packets (LSB first!)
147-150	Management Port TCP TX Packets (LSB first!)
151-154	Management Port TCP Established Connections (LSB first!)
155-158	Management Port TCP Rejected Connections (LSB first!)
159-162	Management Port TCP Closed Connections (LSB first!)
163-166	Management Port TCP Active Connections (LSB first!)
167-170	Management Port TCP Keep Alive Timeout (LSB first!)
171-174	Management Port TCP Retransmit Timeout (LSB first!)
175-178	Management Port TCP Retransmissions (LSB first!)
179-182	Reserved (0x00)
183-186	System Up Time (LSB first!) (in miliseconds)
187-188	Hardware Error (LSB first!) Bit 0 : SDRAM Error Bit 1 : EEPROM Error Bit 2 : FPGA Error Bit 3 : Internal Flash Error

	Bit 4 : Flash 1 Error (Web Server Flash) Bit 5 : Flash 2 Error (Storage Flash) Bit 7..15 : Reserved (0)
189-190	IIC Error (LSB first!) Bit 0 : No ACK received Bit 1 : Address overflow Bit 2 : Polling Error Bit 3..15 : Reserved (0)
191	Test code read from the FPGA (0x5C)
192	FPGA Program Version High
193	FPGA Program Version Low
194	FPGA Status Bit 0 : Basic PLL Locked Bit 1 : Serial PLL Locked Bit 2 : External DCM Locked Bit 3 : External Clock Valid Bit 5..4 : CAM Timer state (00 – Idle, 01 – Armed, 10 - Running) Bit 6 : Streaming ADC Board data Bit 7 : Overload
195	Stream Port Ethernet Status Bit 0 : XGMII RX DCM Locked Bit 1 : XGMII Link Bit 2 : Reserved for internal use (TX Buffer is full) Bit 7..3 : Reserved (0)
196-197	External Clock Frequency in kHz (MSB first)
198	DSLV Lock Status
199-200	Stream Port RX Error Counter (MSB first)
201-202	Stream Port RX Overflow Counter (MSB first) (MSB first)
203-204	Stream Port RX Packet Counter (MSB first)
205	Trigger Status
206-214	Reserved (0x00)
215-218	Status (LSB first!) bit 31..2 – Reserved (0) bit 1 – Storage Flash is busy (1) or free (0) bit 0 – WEB Flash is busy (1) or free (0)
219-	DDToIP Version 1 Instruction Counter (LSB first!)

222	
223-226	DDToIP Version 2 Instruction Counter (LSB first!)
227-230	DDToIP Version 3 Instruction Counter (LSB first!)
231	Reserved (0x00)
232-234	SCB Status Register of the SCB-S1 port
235	Reserved (0x00)
236-238	SCB Status Register of the SCB-S2 port
239	Reserved (0x00)
240-242	SCB Status Register of the SCB-S3 port
243	Reserved (0x00)
244-246	SCB Status Register of the SCB-S4 port
247	Reserved (0x00)
248-250	SCB Status Register of the SCB-S5 port
251	Reserved (0x00)
252-254	SCB Status Register of the SCB-S6 port
255	Reserved (0x00)
256-258	SCB Status Register of the SCB-S7 port
259	Reserved (0x00)
260-262	SCB Status Register of the SCB-S8 port
263	Reserved (0x00)
264-266	SCB Status Register of the SCB-S9 port
267	Reserved (0x00)
268-270	SCB Status Register of the SCB-S10 port
271-274	FUP Checksum
275	FUP In Process
276	Board Temperature (in Celsius)
277-278	Reserved (0x00)

279-280	VDD 3.3V voltage in mV (LSB first!) (Main power supply.)
281-282	VDD 2.5V voltage in mV (LSB first!)
283-284	VDD 1.8V XC voltage in mV (LSB first!) (1.8 V voltage of the Xilinx FPGA.)
285-286	VDD 1.2V ST voltage in mV (LSB first!) (Core voltage of the Stellaris Microcontroller.)
287-288	SCB Controller Version
289-290	Marvell Boot Counter (for internal use, MSB first)
291-292	Marvell register 3.0x8127 (for internal use, MSB first)
293-298	Reserved (0x00)
299-300	Debug State (for internal use, MSB first)
301	WEB Boot Completed (for internal use)
302	Max. Temperature
303-304	Max. VDD 3.3V
305-310	Actual value of the Stream #1 Sample Counter
311-316	Actual value of the Stream #2 Sample Counter
317-322	Actual value of the Stream #3 Sample Counter
323-328	Actual value of the Stream #4 Sample Counter

FUP CHECKSUM

Byte	7	6	5	4	3	2	1	0
7-10	Checksum							

SDRAMPAGE message

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0xFF01					
3-4	Length		0x0402					
5-6	Page Address							
7-1030	Page Data							

SCBDATA message (reply for SCBREADCA)

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0xFF02					
3-4	Length							
5-	SCB Data							

SCBDATA message (reply for SCBREADRA)

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0xFF02					
3-4	Length							
5-6	Register Address							
7-	SCB Data							

FLASHPAGE message

Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0xFF03					
3-4	Length		0x0402					
5-6	Page Address							
7-1030	Page Data							

PDIDATA message

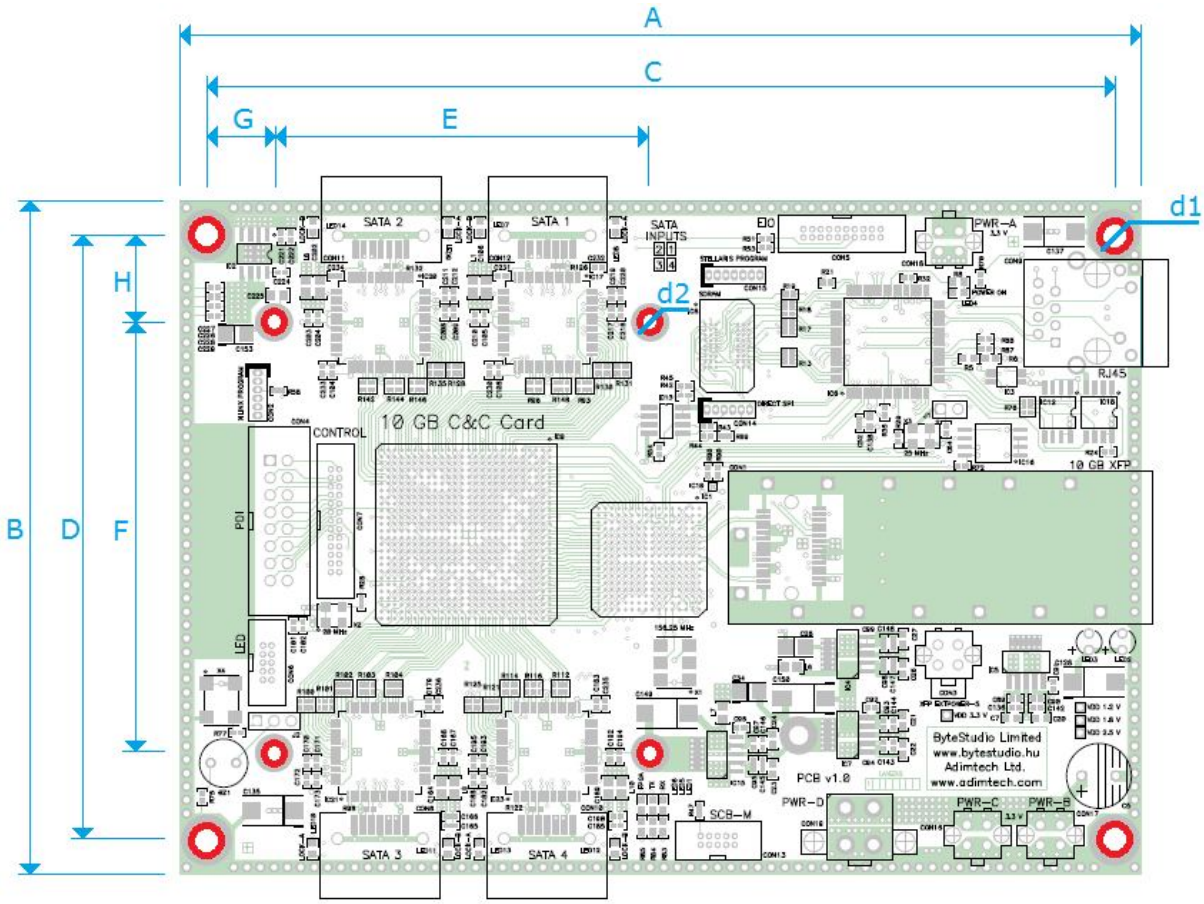
Byte	7	6	5	4	3	2	1	0
1-2	Opcode		0xFF04					
3-4	Length							
5-	Data							

6 Electrical Characteristics

Recommended operating conditions:

Parameter	Min	Typ	Max	Units
VCC (power supply)	3.26	3.3	3.41	V
Input current		3000		mA
Operating temperature	+5		+70	°C

7 Mechanical Dimensions



Units: mm
Tolerance: ±2 %

A	143
B	100
C	135
D	90
E	56
F	64
G	10
H	13
d1	3.5
d2	2.7

Max. height: 20 mm

8 Version Information

Version	Date	Modifications
0.03	23.06.2013	Test versions for development
0.04	01.10.2013	Test versions for development [p] – CAM Timer [p] – Jumbo frames
0.05	14.10.3013	Test versions for development [e] – Serial number corrected in the C&C header [e] – Sample Counter increment [m] – Streamer data FIFO size is 16K [m] – Stream stop condition in fix sample c. mode [p] – Actual values of the sample counters are readable
0.06	24.10.3013	Test versions for development [p] – Serial PLL
1.00	16.01.2014	First official version of the controller [m] – LED and EIO Connector pinout
1.01	16.04.2014	[p] – Firmware Upgrade via UDP [p] – Max. Temperature and VDD 3.3V storage
1.02	02.08.2014	[p] – Dual SATA Mode
1.03	26.02.2015	[p] – Storage flash self test

Keys:
[m] – modification
[e] – error correction
[p] - new feature