LVDS Transport Stream Interface

Version 1.0

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Using this Document

This document is intended for the software and hardware engineer's reference and provides detailed information about the LVDS Transport Stream Interface of the Gigabit Ethernet Controller II. Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact ByteStudio (bytestudio@bytestudio.hu) for additional information that may help in the development process.

Document History

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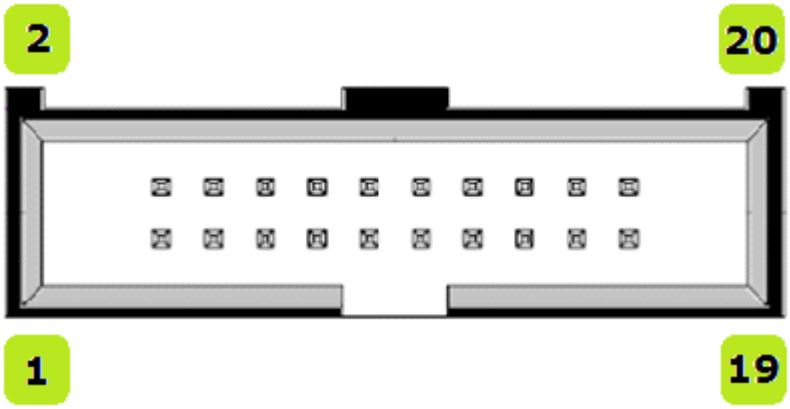
1. LVDS Transport Stream connector

The LVDS Transport Stream connector (input and output) is a 20-pin shrouded header connector made by Samtec (www.samtec.com).



Connector type: Samtec SHF-110-01-L-D-TH

Cable strip: Samtec FFSD-10-01-N

Pin	Description	Direction	IO Standard
1	TS Clock P	In or Out	LVDS
2	TS Clock N	In or Out	LVDS
3	TS Sync P	In or Out	LVDS
4	TS Sync N	In or Out	LVDS
5	TS Data0 P	In or Out	LVDS
6	TS Data0 N	In or Out	LVDS
7	TS Data1 P	In or Out	LVDS
8	TS Data1 N	In or Out	LVDS
9	TS Data2 P	In or Out	LVDS
10	TS Data2 N	In or Out	LVDS
11	TS Data3 P	In or Out	LVDS
12	TS Data3 N	In or Out	LVDS
13	TS Data4 P	In or Out	LVDS
14	TS Data4 N	In or Out	LVDS
15	TS Data5 P	In or Out	LVDS

16	TS Data5 N	In or Out	LVDS
17	TS Data6 P	In or Out	LVDS
18	TS Data6 N	In or Out	LVDS
19	TS Data7 P	In or Out	LVDS
20	TS Data7 N	In or Out	LVDS

2. LVDS levels

LVDS is a differential signaling system. It transmits information as the difference between the voltages on a pair of wires (P and N). The two wire voltages are compared at the receiver. The transmitter injects typically 3.5 mA into one wire (P or N, depending on the logic level to be sent). The current passes through a resistor of about 100 ohms at the receiving end. The voltage difference across the resistor is therefore about 350 mV. The receiver senses the polarity of this voltage to determine the logic level. The common-mode voltage is about 1.25 V.

LVDS Output: V_{OD} = 250-350 mV
V_{OCM} = 1.125-1.375 V

LVDS Input: V_{ID} = 100-600 mV
V_{ICM} = 0.3-2.35 V

3. Signal description

The LVDS TS Interface consists of a clock signal (TS Clock), a sync signal (TS Sync) and an 8-bit width data bus (TS Data). TS Clock runs at the rate at which bytes are offered to the device. Data will be sampled (it must be stable) on the rising edge of the clock signal. TS Clock frequency must be between 0 and 133 MHz.

4. LVDS TS Stream

Using the LVDS TS Interface 188-byte long Transport Stream packets can be transferred from 255 different TS source. The original sync byte (0x47) of the TS packets is replaced by the 8-bit Stream Number (SN). The TS Sync must be high during the Stream Number. The Stream Number is followed by 187 TS data bytes and an optional Tali field. If

there is no Tail field transported (Figure 1.):

- The next packet can follow immediately the previous one without inserting staffing bytes.
- Any staffing byte with value 0x00 can be inserted between the two packets.

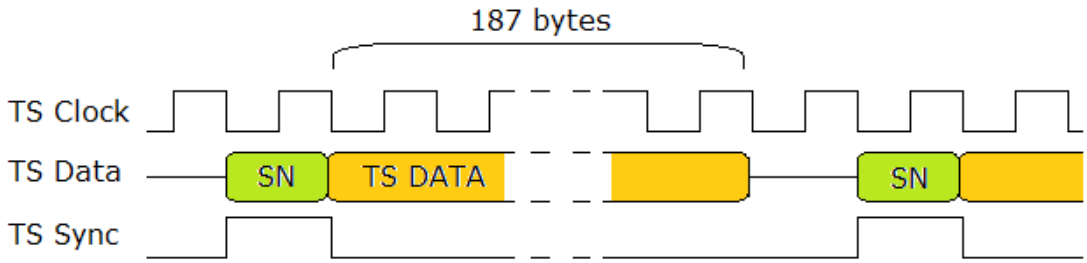


Figure 1. LVDS TS without Tali field and with 1 stuffing byte

If there is Tail field transported (Figure 2.), the 188 TS data bytes are followed by N x 4-byte Tali field. The length of the Tail field is between 4 and 68 bytes (so the maximum length of one extended TS packet is 256 bytes).

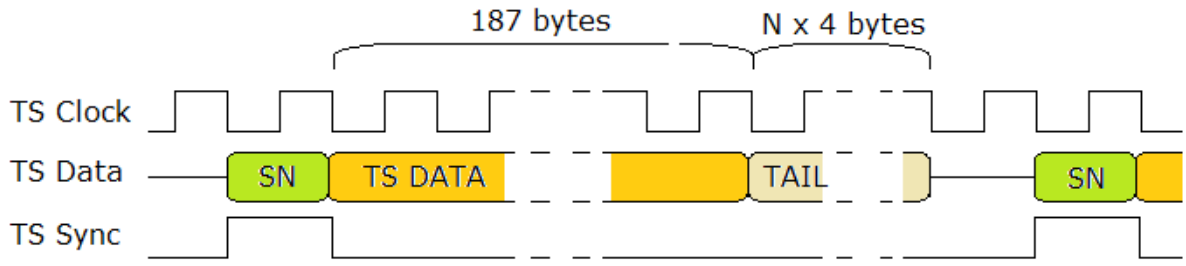


Figure 2. LVDS TS with Tali field and 1 stuffing byte

5. Tail filed

The tail field (Figure 3.) consists of 32-bit long units from T0 to TN (N=0..16). T0 is always present, while T1..T16 are optional. Tx/By represents the y bit of Tx.

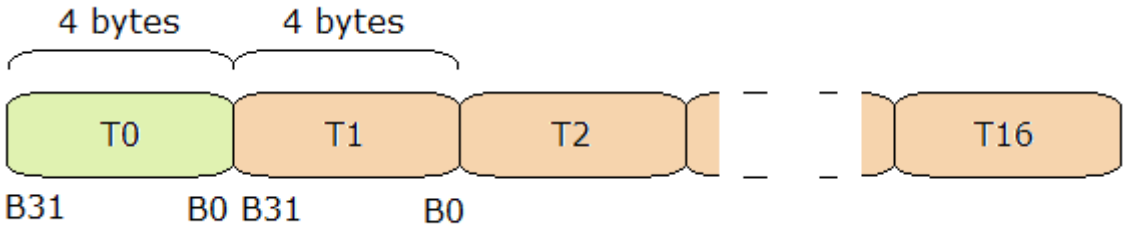


Figure 3. Tail field

Unit	Function
T0	Control
T1	32-bit Packet Counter (PC)
T2	32-bit Packet Arrival Time Stamp (PATS)
T3	23+9 bit PCR format Packet Arrival Time Stamp (PCRTS)
T4	32-bit Source SCB Address (SSCBA)
T5..T16	Reserved

T0 structure:

T0/B31 : 1=Tail field present
T0/B30 : 1=Sync lost event
T0/B29 : 1=Sync error event
T0/B28..T0/B24 : Reserved (0)
T0/B23..T0/B16 : System clock frequency (used to generate Packet Arrival Time Stamp) in MHz.
T0/B15 : 1=T1 unit present
T0/B14 : 1=T2 unit present
...
T0/B0 : 1=T16 unit present

Let's see the following example:

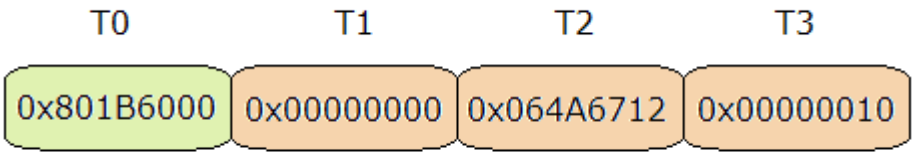


Figure 4. Tail field example

The Tali field present bit in T0 (B31) is set. T0/B23..T0/B16 is 0x1B means that the system clock frequency used to generate Packet Arrival Time Stamp in T2 is 27 MHz. T2 and T3 units are present (T0/B15..T0/B0 is 0x6000), T1 is filled with zeros.

6. Instructions over TS

The Stream Number 255 is reserved for sending instructions between two boards. Stream Numbers from 0 to 254 can be used to transfer TS.