Version 1.03

Instruction Manual

1.03-A

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Using this Document

This document is intended for the software and hardware engineer’s reference and provides detailed information about the Gigabit Ethernet Controller. Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact ByteStudio (bytestudio@bytestudio.hu) for additional information that may help in the development process.

Document History

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1 Introduction

Developing ByteStudio's ASI Remultiplexer & Streamer was based on the possibilities offered by FPGA technology. The ASI Remultiplexer & Streamer represents the latest generation of transport stream remultiplexers.

As one of its remarkable features, the remultiplexer is capable of simultaneously receiving the streams of six different signal sources, and it can be programmed to assemble of them any optional streams. The input stage is capable of enabling, disabling or remapping the PID values of the six input streams, prior to loading the packets in the SDRAM. The ASI Remultiplexer & Streamer uses 128-Mbit SDRAM as temporary storages for the data streams to be inserted. The device can compose one output transport stream. The data rate of the output signal can be set in a very wide range, and as a special feature, the clock signals (data rates) of the inputs can be carried over to the output without any change. The format of the output signal can be set to 188 and 204 bytes/packet. The remultiplexer is equipped with 12 output inserters (with a total of 32 Mbytes flash memory), which allow inserting also own data streams in the output transport stream. These data streams can be tables, still and moving pictures loaded in the memory, set-top box update software or any other information the user may need. The storage capacity of more than 500 Mbits allows applying many new solutions. The output streams can be both SPTS (single program/TS) and MPTS data streams. The large PCR errors occurring in the input line will be corrected by PID, using statistical type PCR correctors of new solution. The statistical type PCR corrector in the output stage performs full error correction at all PID values.

The ASI Remultiplexer & Streamer can be programmed through the Serial Data Interface. In the remultiplexer the communication is handled by the Instruction Manager. The Instruction Manager serves the connected transport stream remultiplexer units. The module provides an RS-232 port and outputs for driving LEDs.

2 Features

- Single 3.3 V power supply
- 6 independent, parallel Transport Stream Inputs (up to 216 Mbps/input)
- Programmable transport stream output frequency (120 Hz – 40.5 MHz) and format (188/204 bytes).
- The Output supported by 128-Mbit SDRAM capacity (65536 packets) and 12 PSI Inserters
- Statistical type PCR Corrector for each PID value (± 500 ns)
- Easy to program via Serial Data Interface
- Extended instruction set (Digital Data Transmission over IP - DDToIP)
- Status and overflow LED ports
- RS-232 Interface (or optional GPS module interface)
- Low power consumption, high reliability, long life time

3 Model List and Block Diagram

ASI Remultiplexer Model List:

Model	Features
6RA	6 parallel Transport Stream Inputs 1 Transport Stream Output 128-Mbit SDRAM

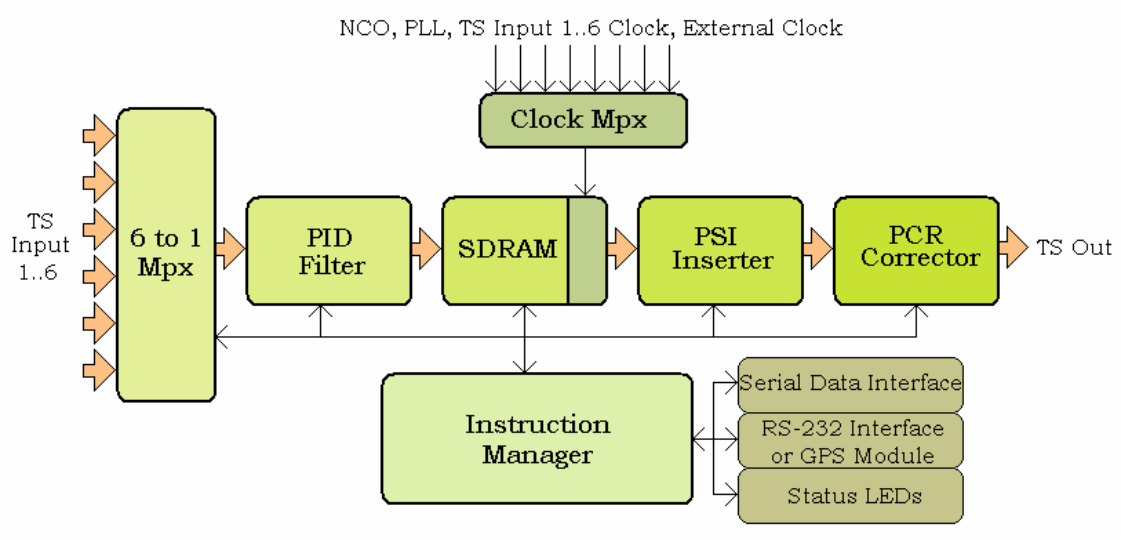


Figure 1. ASI Remultiplexer-6RA Block Diagram

4 General Description

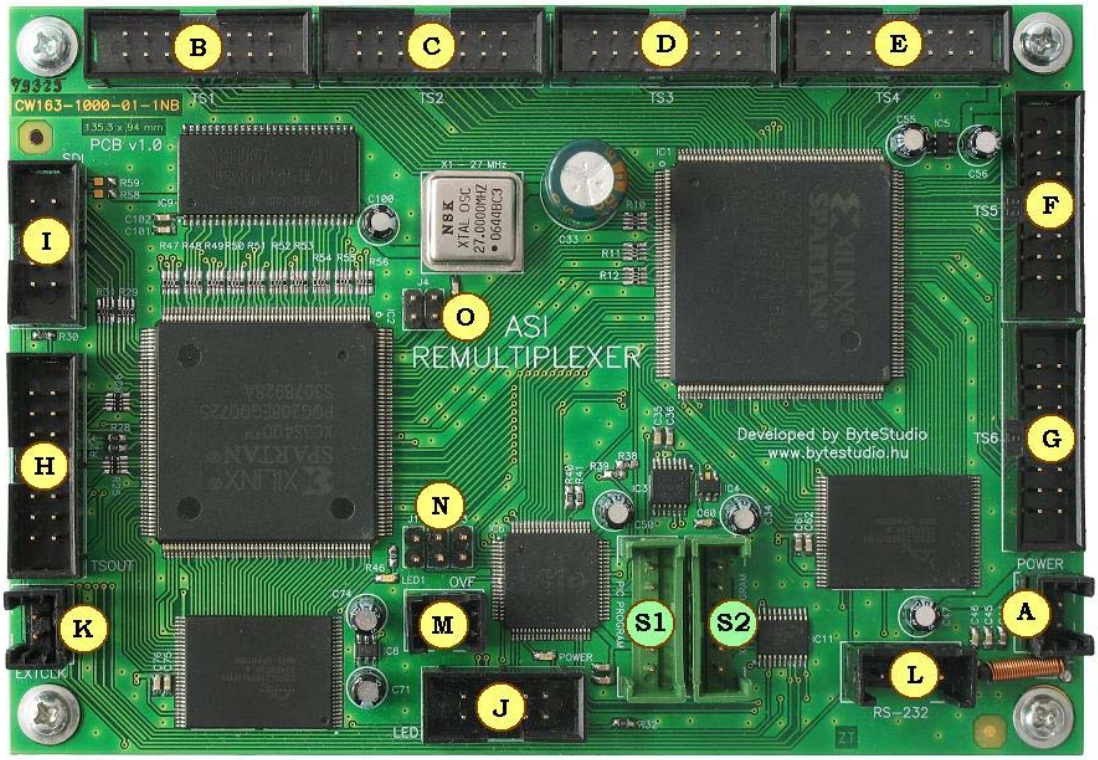


Figure 2. Connectors

Char	Connector
A	POWER (3.3 V)
B	TS1 (Transport Stream Input 1)
C	TS2 (Transport Stream Input 2)
D	TS3 (Transport Stream Input 3)
E	TS4 (Transport Stream Input 4)
F	TS5 (Transport Stream Input 5)
G	TS6 (Transport Stream Input 6)
H	TSOUT (Transport Stream Output)
I	SDI (Serial Data Interface)
J	LED
K	EXTCLK (External Clock Input)
L	RS-232
M	OVF (Overflow LED Output)
N	J1, J2 and J3 Jumpers

O	*Measurement points (Don't connect!))*
S1	*Programming connector (Don't connect!)*
S2	*Programming connector (Don't connect!)*

4.1 Power Supply

The ASI Remultiplexer needs single 3.3 V power supply. Connector (Connector A) pinout:

Pin	Description	Direction
1	GND	
2	Power 3.3 V	Input

Maximum current consumption: 350 mA.

4.2 Device Management

The ASI Remultiplexer can be programmed and controlled via a two-way Serial Data Interface (Connector I), through which data can be loaded from a master device (e.g. a Gigabit Ethernet Controller (BS-GEC, CW-4901)) to the remultiplexer (slave device) or from the remultiplexer to a master device. The Serial Data Interface (SDI) supports the CW-Net compatible serial mode. In this mode operation is fully compatible with the CableWorld CW-4900 Ethernet Controller's Serial Data Interface. For details visit www.cableworld.eu. The pinout of the connector is the following:

Pin	Description (CW-Net compatible serial mode)	Direction	Impedance
1	Serial Read (SR)	OC Output	Weak pullup
2	ENABLE 1	Input	22 Ω
3	ENABLE 2	Input	22 Ω
4	ENABLE 3	Input	22 Ω
5	ENABLE 4	Input	22 Ω
6	ACK	OC Output	Weak pullup
7	RESET	Input	4.7 kΩ pullup
8	Serial Write (SW)	Input	22 Ω
9	Clock (CLK)	Input	22 Ω
10	GND	-	-

The RESET signal is an active low reset, which resets the whole remultiplexer board. The minimum reset period is 10 ms.

A maximum of 15 slave devices can be simultaneously connected to the serial bus. The slave address (1..15) of the remultiplexer can be set using the SETADDRESS instruction. The factory default slave address is 1. Through the Serial Data Interface the user can perform the following actions:

- Write a DDToIP instruction chain to the remultiplexer.
- Read out the 1024-byte Register Table of the remultiplexer.

4.2.1 Writing DDToIP Instructions

The ASI Remultiplexer can be controlled and programmed by sending instructions via the Serial Data Interface to the device. In a single write cycle a maximum amount of 1446 data bytes can be written to the remultiplexer.

During a write cycle three basic actions can be performed on the serial bus: BYTE WRITE, STOP and ACK (see Figure 3).

The BYTE WRITE action:

- Writes 8 serial bits (1 byte, MSB first) to the remultiplexer.
- The master device drives the ENABLE, CLK and SW signals.
- The ENABLE signals refer to the slave address.
- Data on the SW line will be sampled by the remultiplexer on the rising edge of the serial clock (CLK).

The STOP action:

- The master device sets the ENABLE lines to low (ADDRESS 0x0) and generates a clock pulse.

The ACK action:

- The remultiplexer pulls down the ACK line (open collector output).

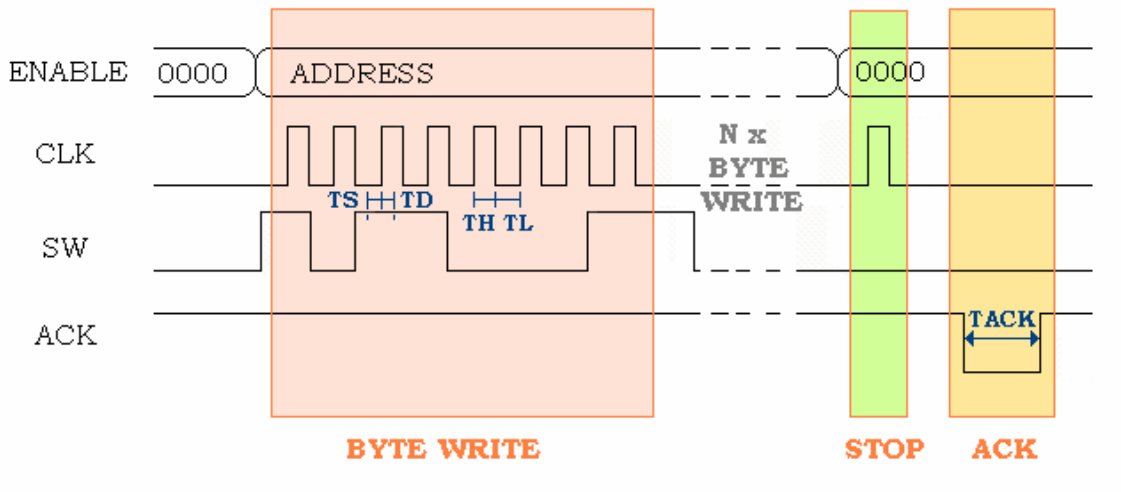


Figure 3. Serial Data Interface write actions

Parameter	Max	Min	Unit
TS (SW data setup time)	-	50	ns
TD (SW data hold time)	-	50	ns
TH (CLK high pulse width)	-	150	ns
TL (CLK low pulse width)	-	150	ns
TACK (ACK pulse width)	750	500	ns

The DDToIP instructions are encapsulated in serial data packets. The sequence of a write cycle is the following (Figure 4):

- The master sets the ENABLE signals to the slave address of the remultiplexer.
- The master writes the 0xAB and 0x6E hexadecimal control bytes (Write Start Code).
- The remultiplexer generates an ACK pulse.
- The master writes the DDToIP data bytes.
- The master sets the ENABLE signals to low and generates a STOP pulse.
- The remultiplexer generates an ACK pulse.

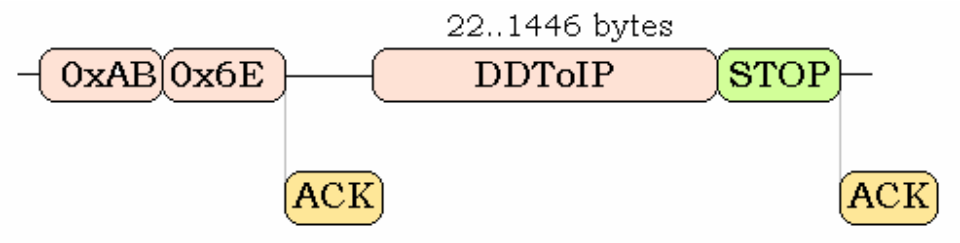


Figure 4. Write cycle (Writing DDToIP Instruction Chain)

4.2.2 DDToIP Protocol

Digital Data Transmission over IP (DDToIP) is a flexible device management protocol specially developed for the Gigabit Ethernet Controller (BS-GEC). The ASI Remultiplexer uses the same protocol. The structure of the DDToIP protocol is shown in Figure 5.

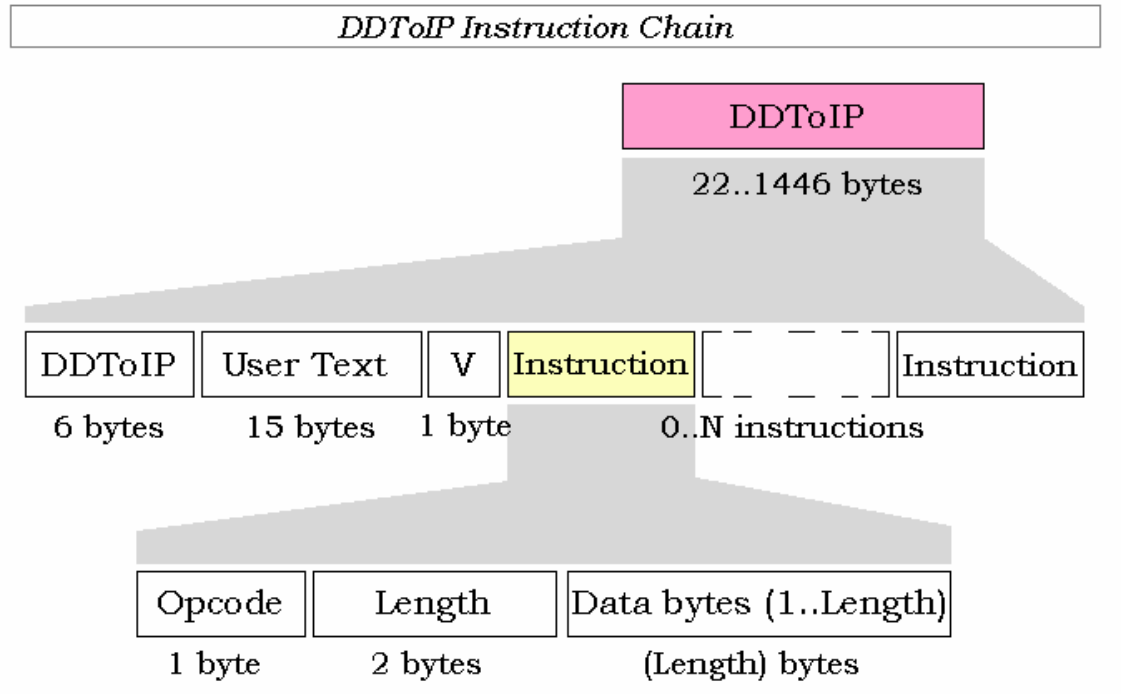


Figure 5. DDToIP Protocol

The data block must start with “DDToIP” characters (44-44-54-6F-49-50 hexadecimal). It is followed by a 15-character user-defined string (User Text). You can use this field to place your company name into the serial data packet. V (version number) must be 0x01. The DDToIP packet can contain one or more instructions. The instructions are performed sequentially. Details are described in section 5.

4.2.3 Reading out the Register Table

The ASI Remultiplexer has a 1024-byte read-only Register Table, which contains information about the device and the remultiplexing process. The Register Table can be read out via the Serial Data Interface. For details about the Register Table see section 5.6.

During a read cycle four basic actions can be performed on the serial bus: BYTE WRITE, BYTE READ, STOP and ACK. The BYTE WRITE, STOP and ACK actions and the timing requirements are the same as described in section 4.2.1.

The BYTE READ action:

- Reads 8 serial bits (1 byte, MSB first) from the remultiplexer.
- The master device drives the ENABLE and CLK lines.
- The ENABLE signals refer to the slave address.
- The remultiplexer drives the SR line. Data on the SR line is changed on the rising edge of the serial clock. Data can be sampled by the master device on the falling edge of the serial clock.

The sequence of the read cycle is the following (Figure 6):

- The master sets the ENABLE signals to the slave address of the remultiplexer.
- The master writes the 0xAB and 0x93 hexadecimal control bytes (Read Start Code).
- The master reads the data bytes (the Register Table from address 0x0000). The Register Table contains 1024 bytes.
- The master sets the ENABLE signals to low and generates a STOP pulse.
- The remultiplexer generates an ACK pulse.

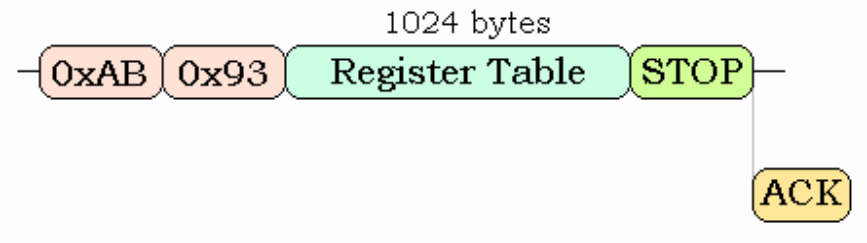
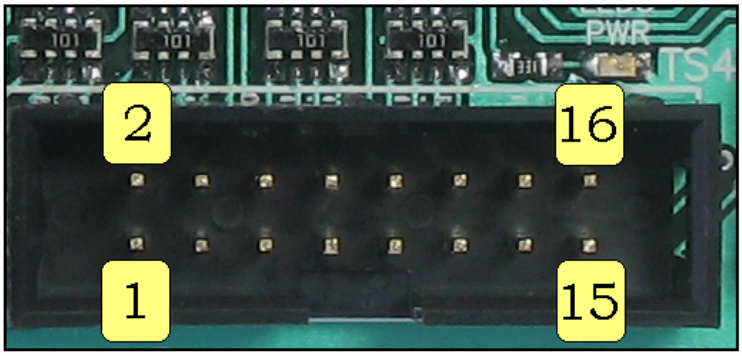


Figure 6. Read cycle

4.3 Transport Stream Input 1 to 6

The ASI Remultiplexer has six transport stream input connectors: TS1, TS2, TS3, TS4, TS5 and TS6 (Connector B to G). The connectors are 16-pin AMP type. The pinout is the following:

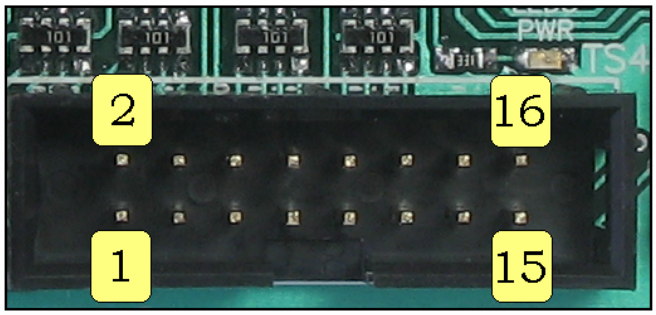


Pin	Description	Direction	Impedance
1	NC (Reserved)	-	-
2	TS Data 0	Input	-
3	TS Data 1	Input	-
4	TS Data 2	Input	-
5	TS Data 3	Input	-
6	GND	-	-
7	Reset	Output	-
8	TS Data 4	Input	-
9	TS Data 5	Input	-
10	TS Data 6	Input	-
11	TS Data 7	Input	-
12	TS Data Valid	Input	-
13	TS Clock	Input	22 Ω
14	GND	-	-
15	VDD (3.3 V)	Output	-
16	GND	-	-

Each Transport Stream Input has an 8-bit data bus (TS Data 0-7); the control signals are TS Clock, TS Data Valid and Reset. The maximum frequency of the TS Clock is 27 MHz. The data changes on the falling edge of the clock signal. If the Data Valid pin is enabled (see the SETGENERALFILTER instruction), TS Data Valid indicates the valid data bytes on TS Data 0-7. Reset (active low) is logic 0 during system reset (see the RESET instruction).

4.4 Transport Stream Output

The ASI Remultiplexer has one Transport Stream Output. The output connector (TSOUT, Connectors H) is a 16-pin AMP type connector. The pinout is the following:



Pin	Description	Direction	Impedance
1	NC (Reserved)	-	-
2	TS Data 0	Output	150 Ω
3	TS Data 1	Output	150 Ω
4	TS Data 2	Output	150 Ω
5	TS Data 3	Output	150 Ω
6	GND	-	-
7	Reset	Output	-
8	TS Data 4	Output	150 Ω
9	TS Data 5	Output	150 Ω
10	TS Data 6	Output	150 Ω
11	TS Data 7	Output	150 Ω
12	NC (Reserved)	-	-
13	TS Clock	Output	150 Ω
14	GND	-	-
15	VDD (3.3 V)	Output	-
16	GND	-	-

The Transport Stream Output has an 8-bit data bus (TS Data 0-7), and the control signals are TS Clock and Reset. The TS Clock frequency refers to the frequency of the selected clock source (NCO, PLL, TS Input Clock 1..6 or External Clock). The data changes on the falling edge of the clock signal.

Reset (active low) is logic 0 during system reset (see the RESET instruction).

4.5 NCO and PLL

The ASI Remultiplexer has an independent user programmable Numeric Controlled Oscillator (NCO). The frequency can be set between 1 Hz and 40.5 MHz in 1 Hz steps. The NCO frequency is derived from the 81 MHz (50 ppm) system clock. The jitter depends on the division ratio. The frequency can be set using the SETNCO instruction.

The board contains a Texas CDCE913 type programmable 1-PLL clock synthesizer with very low period jitter (60 ps). The PLL frequency can be set with the SETPLL instruction between 97753 Hz and 40.5 MHz.

Both the NCO and the PLL can generate clock signal for the Transport Stream Output. To select the output clock source use the SETSTREAMFORMAT instruction.

4.6 Remultiplexer Channel

The ASI Remultiplexer contains a complex remultiplexer channel. The channel consists of the 6 to 1 TS Multiplexer, the PID Filter, the SDRAM, the PSI Inserter and the PCR Corrector (Figure 7). The maximum allowed data rate of the TS inputs is 216 Mbit/sec/input.

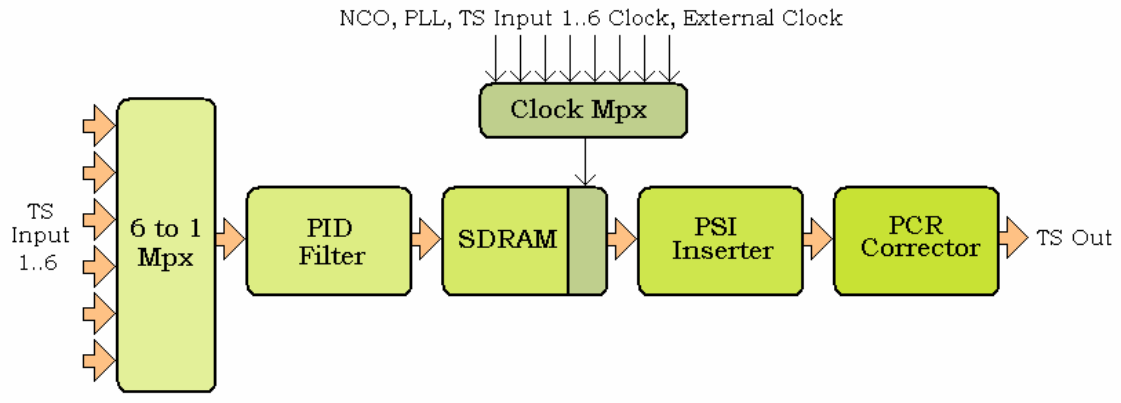


Figure 7. Remultiplexer channel

4.6.1 The General Filters and the PID Filter

The ASI Remultiplexer is capable of simultaneously receiving the streams of six different signal sources. The DVB elementary streams are identified by their input numbers (1..6) and PID values (0..8191).

Each TS input has an own General Filter unit. The General Filters are parts of the 6 to 1 Multiplexer module (Figure 8). The General Filter can enable or disable the TS input (EN) and it finds the sync (SYNC). The General Filter can remove from the stream the null packets (NPF) and packets with TSP Error indicator set to 1 (TSP). The filtering properties can be set using the SETGENERALFILTER instruction.

The PID Filter & Remapper is capable of enabling, disabling or remapping the PID values of the six input streams, prior to loading the packets in the SDRAM. Every transport stream packet is identified by its input number and PID value. The PID Filter & Remapper examines the TS packets and decides to filter or remap them. The remap and filter information is stored in a 16 M x 16-bit Flash Memory. The PID Filter & Remapper computes a memory address from the input number (IN) and PID value of the TS packet. This 16-bit address is used to locate the corresponding filter/remap information (16-bit Filter Data). (Only the lower 64K x 16-bit memory block is used.)

The address algorithm is the following (Figure 9):

- Every TS packet has a 3-bit input number (IN) and a 13-bit PID value.
- Address(23 downto 16) is always zero (0x00).
- Address(15 downto 13) will be the input number minus 1 (IN-1).
- Address(12 downto 0) will be the PID.
- The address locates a 16-bit Filter Data.

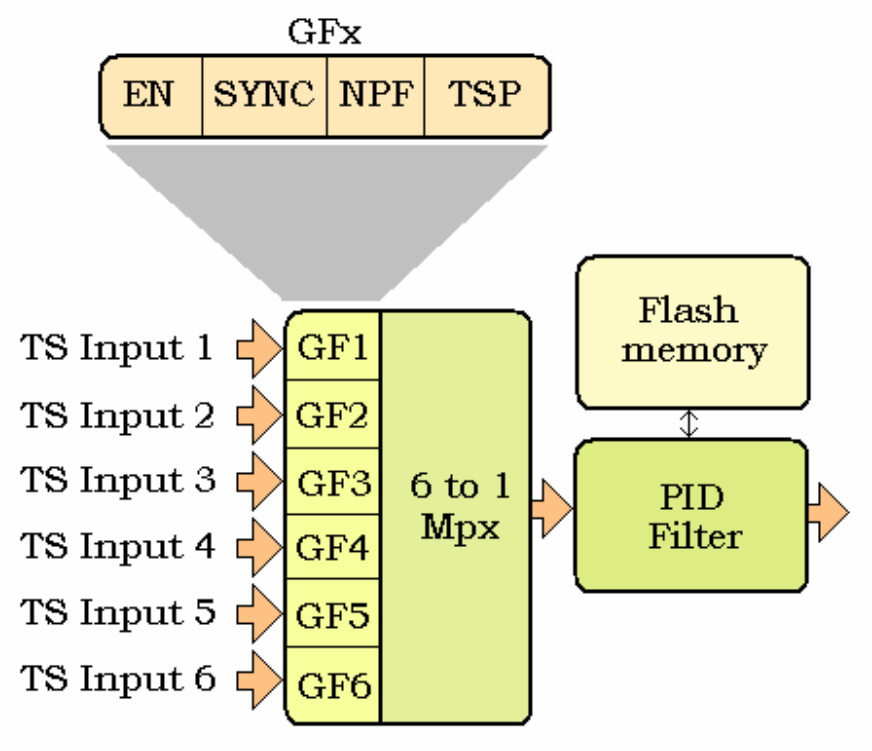


Figure 8. The General Filters and the PID Filter

The PID Filter's Flash Memory can be erased with the ERASEPIDFILTER instruction or the BLOCKERASEPIDFILTER instruction (Block = 0). The user should monitor the corresponding busy flag in the PID Filter State byte (see the Register Table). This flag indicates whether an erase algorithm is in progress ('1') or completed ('0'). The PID Filter can be programmed with the WRITEPIDFILTER instruction. The user can program one Filter Data per instruction, but one DDToIP instruction packet can contain many WRITEPIDFILTER instructions.

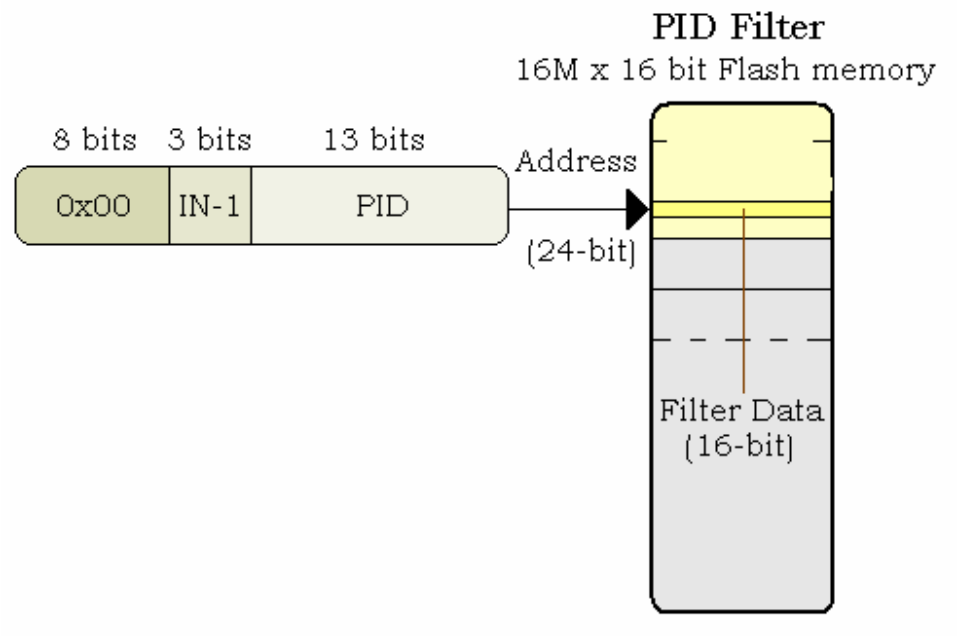


Figure 9. The memory address of the PID Filter

4.6.2 SDRAM

The filtered and remapped TS packets are temporarily stored in a 128-Mbit SDRAM. This SDRAM works as a FIFO memory (Figure 10). The input data rate is determined by the data rate of the TS inputs and the configuration of the PID Filter and can be read out from the Register Table (SDRAM Input Packets / sec). The SDRAM can store 65536 packets as a maximum. If the SDRAM is full the corresponding overflow bit is set (in the Register Table and the LED port).

The output data rate can be programmed between 960 bit/sec and 324 Mbit/sec. The output TS clock can be derived from nine sources:

- The remultiplexer has an internal NCO unit. The NCO's frequency can be set using the SETNCO instruction (120 Hz – 40.5 MHz).
- The board contains a Texas CDCE913 type programmable 1-PLL clock synthesizer. The PLL frequency can be set with the SETPLL instruction (97753 Hz – 40.5 MHz).
- The clock of the TS Input 1 to 6.
- External Clock connector (Connector K)

The user can set the clock source and the output stream format (188-byte or 204-byte) with the SETSREAMFORMAT instruction. The output data rate can be computed from the clock frequency and the stream format. The output of the SDRAM has a null packet inserter. The Register Table contains the number of inserted null packets per seconds.

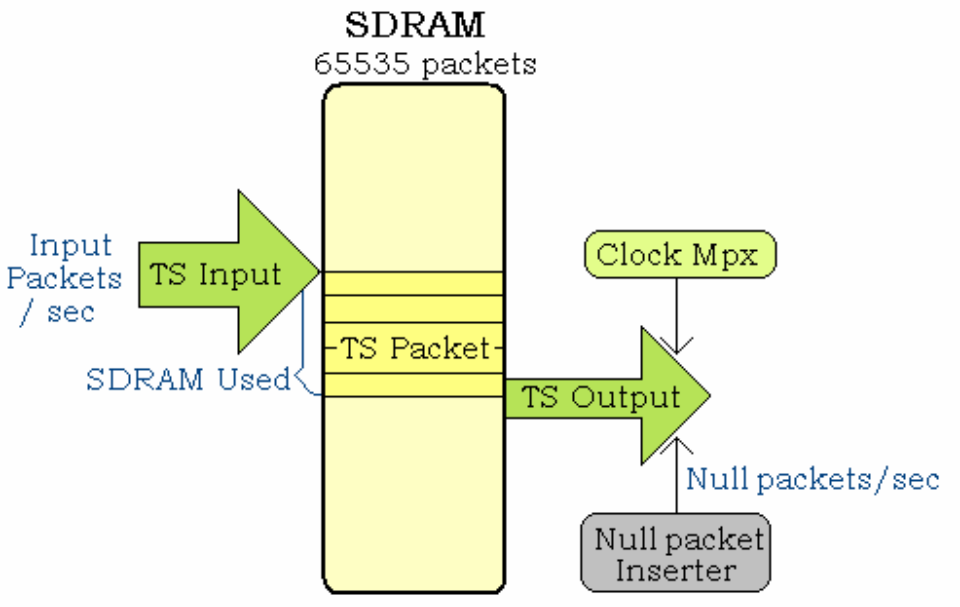


Figure 10. Input and Output streams

4.6.3 Output Inserter

The ASI Remultiplexer is equipped with 12 output inserters (PSI Inserters), which allow inserting also own data streams in the output transport stream. These data streams can be tables, still and moving pictures loaded in the memory, set-top box update software or any other information the user may need.

The Output Inserter unit contains a 32-Mbyte Flash memory, which is divided into 131072 segments. One segment is a 256-byte memory area which stores control information (Timer and ACC in the first 4 bytes), TS packet data (188 or 204 bytes) and user data.

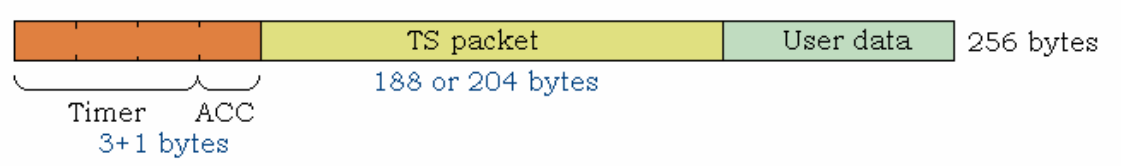


Figure 11. Output Inserter memory segment

All the 256 bytes of the segments can be programmed (see the WRITEPSI instruction), and optional user data can be stored on the last few bytes.

The programmed segments are organized into sectors (Figure 12). The PSI Inserter memory contains 12 independent sectors. Every sector has a programmable start address and end address (see the SETSECTOR instruction). There are no limitations in setting these addresses. The sectors can be enabled or disabled.

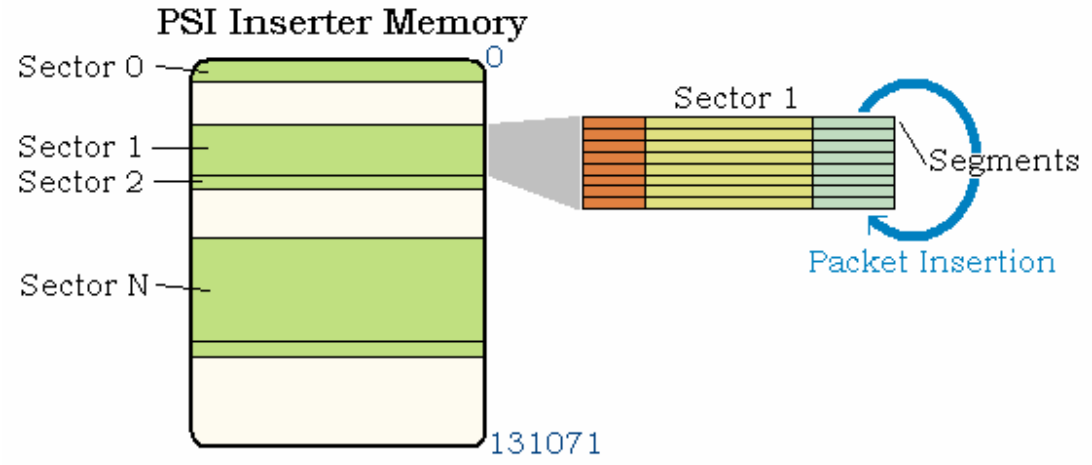


Figure 12. PSI Inserter memory structure

The 12 sectors work independently. The packet insertion starts with the first packet in the sector (start address). The timer value (first 3 bytes of the segment) determines the delay (in 1 ms units) after the packet insertion. After the last packet the insertion is started afresh.
Notes:

- The start address is the address of the first segment, while the end address is the address of the last segment in the sector.
- The start address and the end address can be the same. In this case the sector contains only one segment (packet).

- Timer = 0 means that there is no delay between the packets, so the insertion is continued immediately with the next packet in the sector.

Every segment has an ACC (Auto Continuity Counter) control bit. If the ACC bit is set, the TS packet's continuity counter is automatically incremented after the insertion. *Important: to increment the continuity counter automatically the TS packet's adaptation field control must be 10 or 11.*

4.6.4 PCR Corrector

The PCR errors occurring in the input streams will be corrected by PID, using statistical type PCR correctors of new solution. The statistical type PCR corrector in the output stage performs full error correction at all PID values (± 500 ns). The PCR Corrector has three modes:

- OFF: There is no PCR correction.
- ON: Full PCR correction at all PID values.
- DPR (Direct PCR Restamping): There is no PCR correction, but all PCR values are replaced with the internal PCR counter value. The internal PCR counter is driven by the remultiplexer's own 27 MHz clock.

The modes can be programmed with the SETPCRCORRECTOR instruction. It's recommended to switch on the corrector when the SDRAM is empty or contains less than 100 packets. For the proper correction the following conditions are required:

- The maximum distance between two PCR packets is 650 ms.
- If the PCR error exceeds the 180 ms 64 times in a row the correction algorithm restarts.
- If the SDRAM contains more than 1024 packets the automatic regulation is paused.

4.7 OVFLED Port

The OVFLED port (connector M) can be used to directly drive an overflow LED on the front panel of the device (serial resistors required).

Pin	Description	Direction
1	GND	-
2	OVERFLOW	Output

The OVERFLOW is high (for 1 second) if an overflow event occurs either on a Transport Stream Input, the SDRAM or the PSI Inserter.

4.8 LED Port

The Overflow & State LED port (connector J) is a 10-pin output port on the board used to signal overflow events and stream perception. The Stream pin is set when there are packets on the input of the SDRAM. The overflow sources are the followings:

- TS Input overflow (too many packets arrive at the input)
- SDRAM overflow (SDRAM is full)
- PSI overflow (the output stream doesn't contain enough null packets to perform the insertion)

Pin	Description	Direction
1	TS Input 1 to 6 overflow	Output
2	SDRAM overflow	Output
3	PSI Inserter overflow	Output
4	Stream	Output
5	Reserved	Output
6	Reserved	Output
7	Reserved	Output
8	Power On	Output
9	VDD (3.3 V)	Output
10	GND	-

The port values are refreshed in every second. So, an overflow event causes a high pulse of one second width on the respective pin. The ports can be directly connected to LEDs (serial resistors required).

4.9 Trap Function

The Trap function is under development.

4.10 Jumpers

There are three jumpers on the remultiplexer board: J1, J2 and J3. The function of the jumpers is the following:

Jumper	Function
J1	Direct Address Jumper
J2	Reset Defaults Jumper
J3	*Reserved*

Direct Address Jumper:

By shorting the Direct Address Jumper the slave address of the remultiplexer will be 1 (the SETADDRESS instruction becomes inefficient).

Reset Defaults Jumper:

The user can reset the default settings by shorting the Reset Defaults Jumper. To reset the default settings follow these steps:

- Switch off (to power off state) the device.
- Short the Reset Defaults jumper.
- Switch on the device and wait for 5 seconds (or more).
- Switch off the device again.
- Open the jumper.

Settings changed to:

- Slave address is 1
- TS Inputs enabled
- Data Valid pins disabled
- Null packet filters enabled
- TSP Error Filters disabled
- Output clock source is NCO (3 MHz)

5 Instruction Set

General instructions:

NOP	Opcode = 0x00
RESET	Opcode = 0x01
WAIT	Opcode = 0x02
LASTINSTRUCTION	Opcode = 0x04
SETUSERDATA	Opcode = 0x07

Configuration instructions:

SETSERIAL	Opcode = 0x10
SETTYPE	Opcode = 0x11
SETUSERTEXT	Opcode = 0x12
SETADDRESS	Opcode = 0x14

Network instructions:

SETTRAP	Opcode = 0x26

Transport Stream Output instructions:

SETNCO	Opcode = 0x40

IP Remultiplexer instructions:

SETGENERALFILTER	Opcode = 0xE0	Cmd = 0x10
WRITEPIDFILTER	Opcode = 0xE0	Cmd = 0x11
ERASEPIDFILTER	Opcode = 0xE0	Cmd = 0x12
RESETPIDFILTER	Opcode = 0xE0	Cmd = 0x13
READPIDFILTER	Opcode = 0xE0	Cmd = 0x14
SETPSISECTOR	Opcode = 0xE0	Cmd = 0x20
WRITEPSI	Opcode = 0xE0	Cmd = 0x21
ERASEPSI	Opcode = 0xE0	Cmd = 0x22
BLOCKERASEPSI	Opcode = 0xE0	Cmd = 0x23
RESETPSI	Opcode = 0xE0	Cmd = 0x24
READPSI	Opcode = 0xE0	Cmd = 0x25
SETSTREAMFORMAT	Opcode = 0xE0	Cmd = 0x27
SETPLL	Opcode = 0xE0	Cmd = 0x28
SETPCRCORRECTOR	Opcode = 0xE0	Cmd = 0x30
SETTESTPCRPID	Opcode = 0xE0	Cmd = 0x31

5.1 General Instructions

NOP instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0x00					
2	Length (MSB)		0x00					
3	Length (LSB)		0x00					

Description:

Do nothing.

RESET instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0x01					
2	Length (MSB)		0x00					
3	Length (LSB)		0x02					
4	ResetType		*0x00 – Reserved* 0x01 – System Reset					
5	Reserved (0x00)							

Description:

The System Reset resets the whole remultiplexer. Reset time is 3000 ms.

WAIT instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0x02					
2	Length (MSB)		0x00					
3	Length (LSB)		0x02					
4	WaitX							
5	WaitY							

Description:

Wait before processing the next instruction.

$t_{Wait\ Time}$ = (WaitX * 100) + WaitY [ms]

LASTINSTRUCTION instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0x04					
2	Length (MSB)		0x00					
3	Length (LSB)		0x00					

Description:

This is the last instruction is the chain. This instruction can be followed by any user data byte in the serial data packet.

SETUSERDATA instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0x07					
2	Length (MSB)		0x00					
3	Length (LSB)		0x21					
4	SAVE	0	0	0	0	0	0	0
5-36	UserData (MSB..LSB)							

Description:

UserData is a 32-byte long user programmable memory space. Use the SETUSERDATA instruction to write this memory.

SAVE: 1 – Save the UserData to EEPROM

5.2 Configuration Instructions

SETSERIAL instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0x10					
2	Length (MSB)		0x00					
3	Length (LSB)		0x04					
4	SerialNumber (MSB)							
5	SerialNumber							
6	SerialNumber							
7	SerialNumber (LSB)							

Description:

Set and store the Serial Number. SerialNumber is a 4-byte unsigned integer.

SETTYPE instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0x11					
2	Length (MSB)		0x00					
3	Length (LSB)		0x02					
4	Type (MSB)							
5	Type (LSB)							

Description:

Set and store the Type. Type is a 2-byte unsigned integer.

SETUSERTEXT instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0x12					
2	Length (High)		0x00					
3	Length (Low)		0x0F					
4-18	UserText (15 characters)							

Description:

Set and store the UserText. UserText is a user-defined string in the Register Table.

SETADDRESS instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0x14					
2	Length (High)		0x00					
3	Length (Low)		0x01					
4	Address		1..15					

Description:

Set and store the SDI slave address of the remultiplexer board.

5.3 Network Instructions

SETTRAP instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0x26					
2	Length (MSB)		0x00					
3	Length (LSB)		0x15					
4	TON	SNMP	TIP		TrapPeriod (0..15)			
5			TI1	TO0	TO4	TO3	TO2	TO1
6								
7-22	IP							
23	Port							

Description:

Set and store the Trap function. Trap messages are generated automatically when an unmasked trap source (TX,TO or TI) occurs.

TON: 1/0 – Trap function is on/off

SNMP: 1 – Trap message format is SNMP (Port is 162)
0 – Trap message format is UDP (Port must be set)

TIP: 1/0 – Send Trap to Me/Send Trap to IP

TrapPeriod: $T_{Trap\ period}$ = TrapPeriod + 1 [s]

TOn: 1/0 – Enable/disable Trap on Output Channel n overflow

TI0: 1/0 – Enable/disable Trap on Input Channel 0 overflow

IP: Destination IP address of the Trap message

Port: Destination port of the Trap message in the case of UDP format

5.4 Transport Stream Output Instructions

SETNCO instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0x40					
2	Length (MSB)		0x00					
3	Length (LSB)		0x05					
4	Channel		1					
5	Frequency (MSB)							
6	Frequency							
7	Frequency							
8	Frequency (LSB)							

Description:

Set and store the NCO frequency. Frequency is a 4-byte unsigned integer in Hz. (The NCO can be the clock frequency of the Transport Stream Output.)

$Frequency_{min}$ = 120 Hz

$Frequency_{max}$ = 40500000 Hz = 40.5 MHz

5.5 Remultiplexer Instructions

SETGENERALFILTER instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0xE0					
2	Length (MSB)		0x00					
3	Length (LSB)		0x05					
4	Cmd		0x10					
5	0	0	EN6	EN5	EN4	EN3	EN2	EN1
6	0	0	DV6	DV5	DV4	DV3	DV2	DV1
7	0	0	NF6	NF5	NF4	NF3	NF2	NF1
8	0	0	TF6	TF5	TF4	TF3	TF2	TF1

Description:

Set the General Filters of the remultiplexer. The settings are valid for all input packets.

ENx: 1/0 – TS Input X enabled/disabled

DVx: 1/0 – TS Input X Data Valid pin enabled/disabled

NFx: 1/0 – Null Packet Filter (remover) on/off

TFx: 1/0 – Transport Error Filter (remover) on/off

WRITEPIDFILTER instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode 0xE0							
2	Length (MSB) 0x00							
3	Length (LSB) 0x08							
4	Cmd 0x11							
5	0	0	0	0	0	0	0	1
6-7	Input Select 0x0000 (TS Input 1) 0x0001 (TS Input 2) 0x0002 (TS Input 3) 0x0003 (TS Input 4) 0x0004 (TS Input 5) 0x0005 (TS Input 6)							
8-9	PID (MSB..LSB)							
10	UD	1	PD	Remap PID (MSB)				
11	Remap PID (LSB)							

Description:

Program the PID Filter. The Filter Data (byte 10 and 11) is stored in the PID Filter's flash memory. Input Select word selects the input channel to be programmed. PID must be between 0 and 8191.

Remap PID: if you don't want to remap, set the Remap PID to the same as the PID.

PD : 1 – PID Disabled (Filter on)
0 – PID Enabled (Filter off)

UD : User defined value

ERASEPIDFILTER instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode 0xE0							
2	Length (MSB) 0x00							
3	Length (LSB) 0x02							
4	Cmd 0x12							
5	0	0	0	0	0	0	0	1

Description:

Erase the PID Filter.

RESETPIDFILTER instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0xE0					
2	Length (MSB)		0x00					
3	Length (LSB)		0x02					
4	Cmd		0x13					
5	0	0	0	0	0	0	0	1

Description:

Reset the PID Filter.

READPIDFILTER instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0xE0					
2	Length (MSB)		0x00					
3	Length (LSB)		0x06					
4	Cmd		0x14					
5	0	0	0	0	0	0	0	1
6-7	Input Select		0x0000 (TS Input 1) 0x0001 (TS Input 2) 0x0002 (TS Input 3) 0x0003 (TS Input 4) 0x0004 (TS Input 5) 0x0005 (TS Input 6)					
8-9	PID (MSB..LSB)							

Description:

Read the PID Filter. PID must be between 0 and 8191 (where PID *mod* 8 = 0). The Input Select and the PID values determine the start address. Data read from the PID Filter (128 Filter Data) can be read out from the Register Table (Readback Data) when Readback Type = 0x01.

BLOCKERASEPIDFILTER instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0xE0					
2	Length (MSB)		0x00					
3	Length (LSB)		0x03					
4	Cmd		0x16					
5	WAIT	0	0	0	0	0	0	1
6	Block (0..255)							

Description:

Erase one block in the PSI Inserter's flash memory. The typical block erase time is 500 ms, the maximum is 3500 ms. The PSI Inserter consists of 256 blocks.

WAIT: 1 – Wait while the erase is finished before executing the next instruction (max. wait time is 4000 ms).

0 – Don't wait.

SETPSISECTOR instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode 0xE0							
2	Length (MSB) 0x00							
3	Length (LSB) 0x09							
4	Cmd 0x20							
5	0	0	0	0	0	0	0	1
6	EN	AS	SAVE	0	Sector (0..11)			
7-9	StartAddress (MSB..LSB)							
10-12	EndAddress (MSB..LSB)							

Description:

Set the PSI Inserter's Sector Table. The StartAddress is the address of the first packet in the sector. The EndAddress is the address of the last packet in the sector. Both the StartAddress and the EndAddress must be between 0 and 131071. If the sector contains only one TS packet, StartAddress and EndAddress are the same. Otherwise EndAddress is larger then StartAddress.

EN: 1 – Sector is enabled
0 – Sector is disabled

AS: 1 – Set StartAddress and EndAddress
0 – Don't set StartAddress and EndAddress

SAVE: 1 – Save to EEPROM
0 – Don't save to EEPROM

WRITEPSI instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode 0xE0							
2	Length (MSB) 0x00							
3	Length (LSB) 0xC5 or 0xD5 (typically)							
4	Cmd 0x21							
5	0	0	0	0	0	0	0	1
6-8	Address (MSB..LSB)							
9-11	Timer (MSB..LSB)							
12	0	0	0	0	0	0	0	ACC
13-n	Transport Stream Packet (188 or 204 bytes)							

Description:

Program the PSI Inserter's flash memory. Address must be between 0 and 131071. Timer value determines the delay (in 1 ms units) after the packet is inserted. Timer = 0 means that there is no delay between the packets, so the insertion is continued immediately with the next packet in the sector. (Length can be between 0x09 and 0x105.)

ACC: 1 – Automatic Continuity Counter enabled
0 – Automatic Continuity Counter disabled

ERASEPSI instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode 0xE0							
2	Length (MSB) 0x00							
3	Length (LSB) 0x02							
4	Cmd 0x22							
5	0	0	0	0	0	0	0	1

Description:

Erase the PSI Inserter's flash memory. The typical chip erase time is 128 seconds, the maximum is 512 seconds. After an ERASEPSI instruction the Busy bit in the PSI State byte (see the Register Table) is set. The Busy bit will be cleared when the erase is finished.

BLOCKERASEPSI instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0xE0					
2	Length (MSB)		0x00					
3	Length (LSB)		0x03					
4	Cmd		0x23					
5	WAIT	0	0	0	0	0	0	1
6	Block (0..255)							

Description:

Erase one block in the PSI Inserter's flash memory. The typical block erase time is 500 ms, the maximum is 3500 ms. The PSI Inserter consists of 256 blocks.

WAIT: 1 – Wait while the erase is finished before executing the next instruction (max. wait time is 4000 ms).

0 – Don't wait.

RESETPSI instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0xE0					
2	Length (MSB)		0x00					
3	Length (LSB)		0x02					
4	Cmd		0x24					
5	0	0	0	0	0	0	0	1

Description:

Reset the PSI Inserter's flash memory (software reset).

READPSI instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0xE0					
2	Length (MSB)		0x00					
3	Length (LSB)		0x05					
4	Cmd		0x25					
5	0	0	0	0	0	0	0	1
6-8	StartAddress (MSB..LSB)							

Description:

Read the PSI Inserter's flash memory. StartAddress must be between 0 and 131071. Data read from the PSI Inserter (256 data bytes, 1 packet) can be read out from the Register Table (Readback Data) when Readback Type = 0x02.

SETSTREAMFORMAT instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode		0xE0					
2	Length (MSB)		0x00					
3	Length (LSB)		0x03					
4	Cmd		0x27					
5	0	0	0	0	0	0	0	1
6	F	0	PSIP	0	Clock Source			

Description:

Set the remultiplexer output stream parameters.

F: 1 – 188-byte format.
0 – 204-byte format.

Clock Source: 0x0 - NCO
0x1 - PLL
0x2 - TS Input 1
0x3 - TS Input 2
0x4 - TS Input 3
0x5 - TS Input 4
0x6 - TS Input 5
0x7 - TS Input 6
0x8 - External Clock

PSIP: 1 – High PSI Inserter priority.
0 – Low PSI Inserter priority. (If the output stream doesn't contain enough null packets to perform the insertion, the insertion is paused and the PSI Overflow bit and the PSI Overflow LED are set.)

SETPLL instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode 0xE0							
2	Length (MSB) 0x00							
3	Length (LSB) 0x08							
4	Cmd 0x28							
5	Channel 0x01							
6	0	0	0	0	0	0	PDIV (bit 9..8)	
7	PDIV (bit 7..0)							
8	N (bit 11..4)							
9	N (bit 3..0)				R (bit 8..5)			
10	R (bit 4..0)					Q (bit 5..3)		
11	Q (bit 2..0)			P (bit 2..0)			VCO Range	

Description:

Set the PLL-based clock synthesizer (Texas CDCE913). For the parameter (PDIV, N, R, Q, P and VCO Range) values see the CDCE913's data sheet (SCAS849A-JUNE 2007, f_{IN} = 27 MHz).

SETPCRCORRECTOR instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode			0xE0				
2	Length (MSB)			0x00				
3	Length (LSB)			0x02				
4	Cmd			0x30				
5	0	0	0	DPR	0	0	0	ON

Description:

Set the PCR Corrector.

ON: 1 – PCR Corrector On.
0 – PCR Corrector Off.

DPR: 1 – Direct PCR Restamping (if ON = 1).
0 – Normal PCR Correction (if ON = 1).

SETTESTPCRPID instruction

Byte	7	6	5	4	3	2	1	0
1	Opcode			0xE0				
2	Length (MSB)			0x00				
3	Length (LSB)			0x04				
4	Cmd			0x31				
5	0	0	0	0	0	0	0	1
6-7	PCRPID							

Description:

PCRPID must be between 0 and 8191. This instruction is reserved for testing the device.

5.6 ASI Remultiplexer Register Table

Register Table

Byte	7	6	5	4	3	2	1	0
0	0x45							
1	DeviceCode 0x1A							
2-8	Reserved (0x00)							
9-23	User Text (MSB..LSB)							
24-25	Type (MSB..LSB)							
26-29	Serial Number (MSB..LSB)							
30	Address bit 7: Address is set to 1 by the J1 Jumper (1) bit 6..0: SDI address 1..15							
31	Instruction Packet Counter The counter is automatically incremented after an instruction packet (DDToIP instruction chain) is processed.							
32	Version High (VH)							
33	Version Low (VL) VH and VL determine the remultiplexer's version number in VH.VL format. VL can be between 0 and 99 (in decimal format). If VH = 1 and VL = 0 version is 1.00. If VH = 3 and VL = 10 version is 3.10.							
34	TS Input Enable bit 7..6: Reserved bit 5: TS Input 6 enabled (1) / disabled (0) bit 4: TS Input 5 enabled (1) / disabled (0) bit 3: TS Input 4 enabled (1) / disabled (0) bit 2: TS Input 3 enabled (1) / disabled (0) bit 1: TS Input 2 enabled (1) / disabled (0) bit 0: TS Input 1 enabled (1) / disabled (0)							
35	Data Valid Pin Control bit 7..6: Reserved bit 5: TS Input 6 DV pin enabled (1) / disabled (0) bit 4: TS Input 5 DV pin enabled (1) / disabled (0) bit 3: TS Input 4 DV pin enabled (1) / disabled (0) bit 2: TS Input 3 DV pin enabled (1) / disabled (0) bit 1: TS Input 2 DV pin enabled (1) / disabled (0) bit 0: TS Input 1 DV pin enabled (1) / disabled (0)							
36	Null Packet Filter bit 7..6: Reserved bit 5: TS Input 6 Null Packet Filter on (1) / off (0)							

	bit 4: TS Input 5 Null Packet Filter on (1) / off (0) bit 3: TS Input 4 Null Packet Filter on (1) / off (0) bit 2: TS Input 3 Null Packet Filter on (1) / off (0) bit 1: TS Input 2 Null Packet Filter on (1) / off (0) bit 0: TS Input 1 Null Packet Filter on (1) / off (0)
37	TSP Error Filter bit 7..6: Reserved bit 5: TS Input 6 TSP Error Filter on (1) / off (0) bit 4: TS Input 5 TSP Error Filter on (1) / off (0) bit 3: TS Input 4 TSP Error Filter on (1) / off (0) bit 2: TS Input 3 TSP Error Filter on (1) / off (0) bit 1: TS Input 2 TSP Error Filter on (1) / off (0) bit 0: TS Input 1 TSP Error Filter on (1) / off (0)
38	Output Format and Clock Source bit 7: Output Format 188 (1) / 204 (0) bit 6: Reserved bit 5: PSI Inserter priority high (1) / low (0) bit 4: Reserved bit 3..0: Clock Source 0x0 - NCO 0x1 – PLL 0x2 – TS Input 1 0x3 – TS Input 2 0x4 – TS Input 3 0x5 – TS Input 4 0x6 – TS Input 5 0x7 – TS Input 6 0x8 – External Clock
39	IIC Error
40-43	NCO Frequency (MSB..LSB) in Hz
44-49	PLL Data (PDIV,N, R, Q, P, VCO Range)
50	PID Filter State bit 7..1: Reserved bit 0: PID Filter flash busy (1)
51	Internal Read Error Counter (Used for device test.)
52	Readback Type 0x01 – PID Filter Data 0x02 – PSI Inserter Data Others - Unknown
53	Overflow and State LEDs (see section 4.8) bit 7: Power On (1) bit 6..4: Reserved bit 3: Stream (1) bit 2: PSI Inserter overflow (1)

	bit 1: SDRAM overflow (1) bit 0: TS Input 1 to 6 overflow (1)
54	PSI Inserter State bit 7..2: Reserved (000000) bit 1: PSI Inserter overflow (1) bit 0: PSI Inserter flash busy (1)
55	PCR State bit 7..5: Reserved bit 4: DPR on (1) / off (0) bit 3..1: Reserved bit 0: PCR Corrector on (1) / off (0)
56-57	PCR Test PID (Used for device test.)
58	Xilinx Spartan Program Version (MPX – XC3S500E)
59	Xilinx Spartan Program Version (SPP – XC3S400)
60	Model: 0 – ASIR-6RA for WISI Communications 1 – ASIR-6RA for CableWorld
61-63	Reserved (0x00)
64-95	User Data (MSB..LSB) Use the SETUSERDATA instruction to store the User Data.
96	TS Input 1 Sync Error Counter
97-99	TS Input 1 bit 23: Input Stream Format (188 (1) / 204 (0)) bit 22: Input Stream Overflow (1) bit 21..20: Reserved (00) bit 19..0: Input Packets / sec
100	TS Input 2 Sync Error Counter
101-103	TS Input 2
104	TS Input 3 Sync Error Counter
105-107	TS Input 3
108	TS Input 4 Sync Error Counter
109-111	TS Input 4
112	TS Input 5 Sync Error Counter
113-115	TS Input 5
116	TS Input 6 Sync Error Counter
117-119	TS Input 6
120-122	SDRAM Input Packets / sec (bit 19..0) bit 23..20: Reserved (0000)
123	SDRAM State bit 7: SDRAM Overflow after Reset (1) bit 6: SDRAM Overflow (1) bit 5: PCR Correction Pause (1) bit 4..0: Reserved

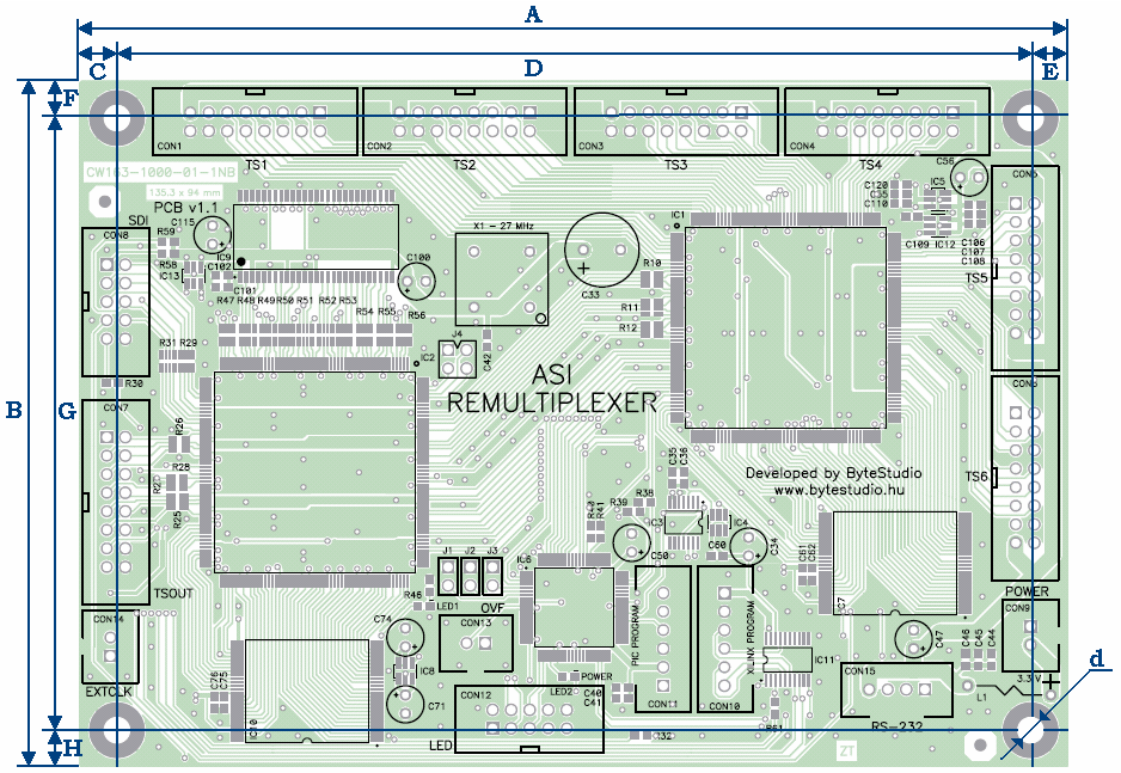
124-125	SDRAM Used (MSB..LSB)
126-128	SDRAM Output Null Packets / sec (bit 19..0) bit 23..20: Reserved (0000)
129-131	Inserted Packets / sec (bit 19..0) bit 23..20: Reserved (0000)
132	PCR Corrector PCR Discontinuity Counter
133-134	PCR Corrector Number of PCRPIDs
135-136	PCR Corrector PCR Base Error (Used for device test.) bit 15: Correction direction +(1) / -(0) bit 14..0: PCR Base (lower 15 bit) Error
137-138	PCR Corrector 1 Test PCRPID Slide (Used for device test.)
139	PCR Corrector 1 Big Error Counter (Used for device test.)
140	PCR Corrector 1 New PCRPID Counter
141-159	Reserved (0x00)
160	Sector 0 bit 7: Sector enabled (1) / disabled (0) bit 6..2: Reserved (00000) bit 1: Start address bit 16 bit 0: End address bit 16
161-162	Sector 0 Start address (bit 15..0)
163-164	Sector 0 End address (bit 15..0)
165-169	Sector 1
170-174	Sector 2
175-179	Sector 3
180-184	Sector 4
185-189	Sector 5
190-194	Sector 6
195-199	Sector 7
200-204	Sector 8
205-209	Sector 9
210-214	Sector 10
215-219	Sector 11
220-767	Reserved (0x00)
768-1023	Readback Data

6 Electrical Characteristics

Recommended operating conditions:

Parameter	Min	Typ	Max	Units
VCC (power supply)	3.25	3.3	3.43	V
Input current		200	350	mA
Operating temperature	0		+70	°C

7 Mechanical Dimensions



Units: mil [mm]

Tolerance: ±2 %

A	5325 [135]
B	3700 [94]
C	200
D	4925
E	200
F	200
G	3400
H	200
d	138 [3.5]

Max. height: 800

8 Version Information

Version	Date	Modifications
1.00	02.04.2008	Version start. Test version for development.
1.01	01.06.2008	First official version of the remultiplexer.
1.02	08.08.2008	[m] New NCO algorithm (1 Hz – 40.5 MHz).
1.03	09.11.2008	[e] PSI Inserter and Sector Write bug fixed.

Keys:
[m] – modification
[e] – error correction
[p] - new feature